Comprehensive Power Backup Solution for Utilizations of Supercapacitors

Quickly Introduction

In today's world, ensuring data integrity and safety under all conditions is emerging as a critical concern. The supercapacitor offers key benefits for rugged environments, high backup power, standby duration, and extended cycles. It's becoming popular in various applications needing dependable backup power. For optimal performance, a reliable, adaptable power management solution is vital.

The LS0502SCD33 (dual channel solution) and the LS0502SCD33S (single channel solution) offer fully integrated power management solutions tailored for systems with supercapacitor backup power applications. They are all-in-one, single-chip power management solutions, especially for supercapacitor backup power applications. They include various features such as input overvoltage and overcurrent protection, a reverse blocking switch, and a supercapacitor charging control circuit with active cell balancing (LS0502SCD33 only). These designs ensure safe, efficient, and cost-effective solution for these applications, all packed into a compact design.

Table 1. Overview Insights of LS0502SCD33 and LS0502SCD33S

Input Overvoltage Protection	OVP = 6 V
Input Maximum Rating	18 V
Input Overcurrent Protection	Input short circuit and overload protection
Reverse Current Blocking	No need extra schottky diode for lower power consumption
2.5 µA low quiescent current	Low power consumption
Power Fault Indicator	Real time monitor
Cell Balance	Active cell balance method (LS0502SCD33 only)
Super Capacitor Short Cuicuit Protection	Maximize supercapacitor lifespan
Program Charger Current	
Program Charger Voltage	
Automatic Main / Balckup Switchover	Seamless and automatically switchover with initerruption
DFN3x3-10L	Low profile package

Figure 1 illustrates the block diagram of LS0502SCD33, showcasing its compact DFN 3X3 package that integrates three low Rdson power devices and an extensive control and protection system. These power devices enable LS0502SCD33 to offer various essential functions, including input overvoltage and overcurrent protection, reverse blocking during backup operation, and a dependable supercapacitor management function. Figure 2 demonstrates how a well-protected power system with dual cell supercapacitor backup can be easily achieved using only external resistors and capacitors.

Figure 1. Functional block diagram (LS0502SCD33)

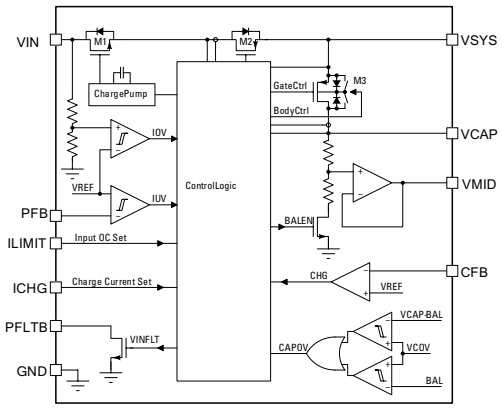
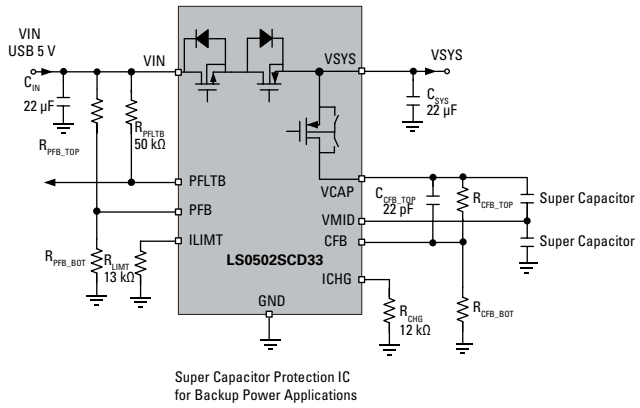


Figure 2. Typical application (LS0502SCD33)

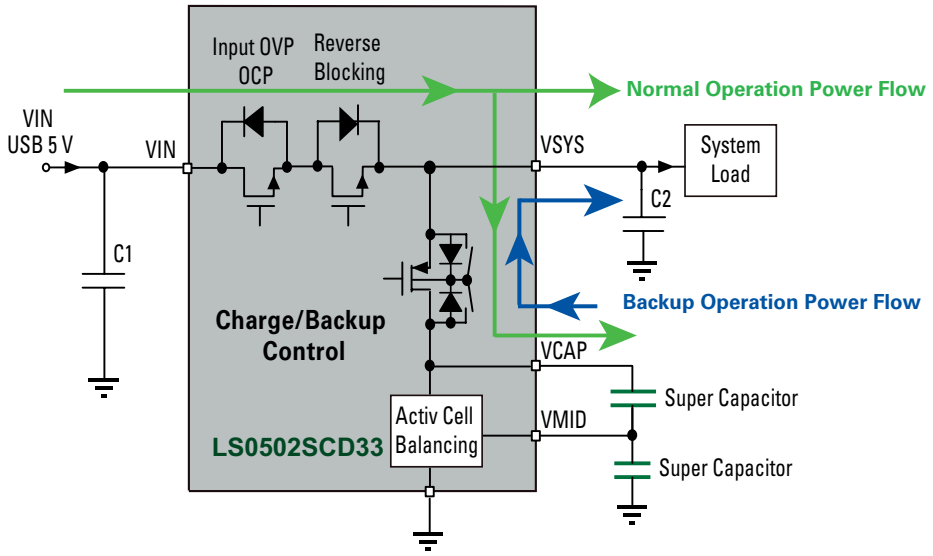


Super Capacitor Protection IC for Backup Power Applications

Meanwhile, Figure 3 illustrates the power flow path during normal and backup operation modes. During normal operation, the system load receives power from the input source while the supercapacitor is automatically charged with a controlled current and voltage level from the input power.

However, in the event of input power loss, LS0502SCD33 or LS0502SCD33S automatically transitions into backup operation mode and generates a fault signal, PFLTB, to inform the system of the input power failure. In this backup mode, the power supply is automatically switched to the supercapacitor, ensuring a reliable backup power source.

Figure 3. Supercapacitor backup power system operation diagram (LS0502SCD33 as an example)



Input Overvoltage/Overcurrent Protection-HV Load Switch (M1 in Figure 3)

In any system, the capacitor starts in a discharged state. The supercapacitor acts as a low-value resistor upon applying the supply voltage, which may lead to a significant inrush current (see Figure 4 and 5 below for example). Without proper control or limitation of this current, it could cause damage. Hence, these circuits require protection against short circuits, over-voltage, and excessive current flow to safeguard the following system.

Figure 4. Load switch (M1 in Figure 3) integrated input overvoltage and overcurrent protection

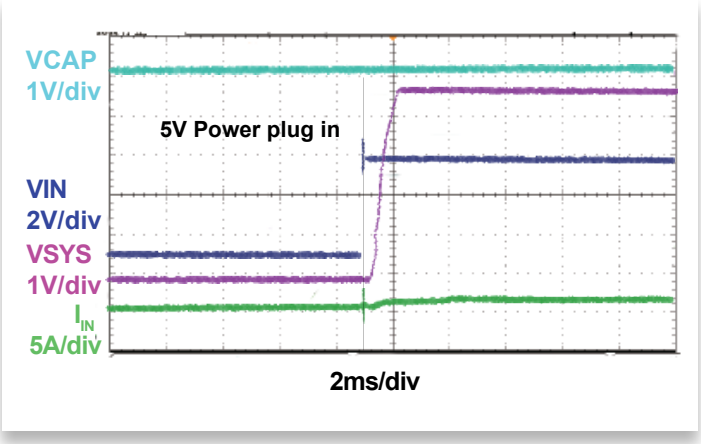
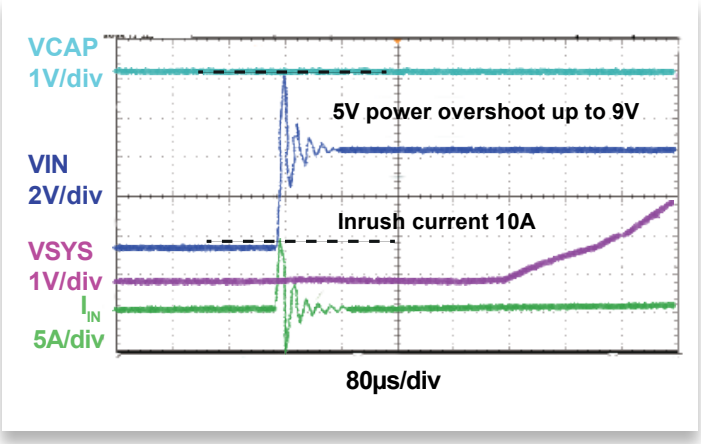


Figure 5. Load switch (M1 in Figure 3) integrated input overvoltage and overcurrent protection (the zoom-in detail of figure 4)



To overcome this, LS0502SCD33 or LS0502SCD33S includes a programmable Input voltage monitor. This monitor activates when the input voltage falls below a specific threshold set by a resistor divider connected to the PFB pin. As a result, a flag signal on PFLTB is triggered, alerting the following system about the event. This alert enables the system to take preventive actions, such as processing and saving data in DRAM, to avoid data loss or potential damage.

Figure 6.
PFLTB indicator-PFLTB goes low when the PFB drop below 1.2 V

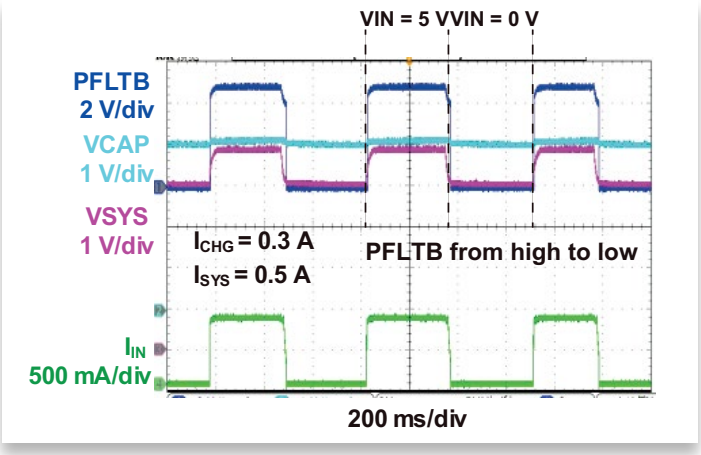
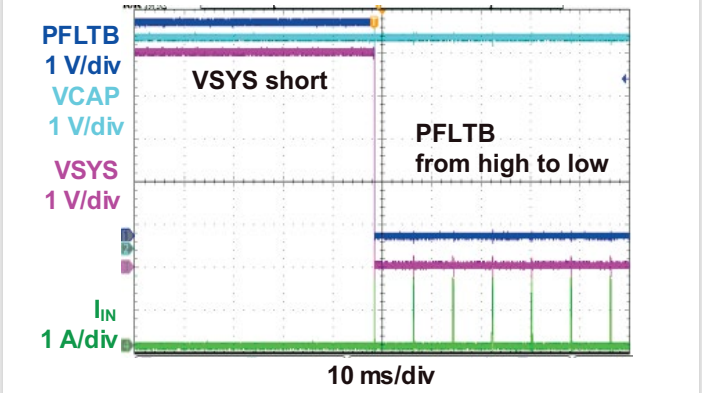


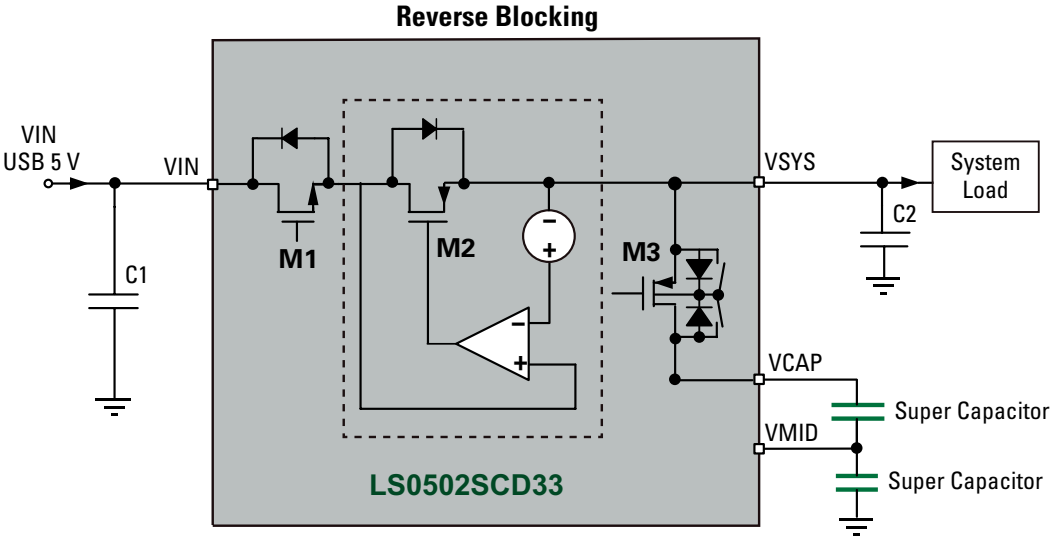
Figure 7.
PFLTB indicator-PFLTB goes low when (VIN-VSYS) exceeds 360 mV



Reverse Blocking Protection – Ideal Diode (M2 in Figure 8)

Furthermore, LS0502SCD33 or LS0502SCD33S includes an ideal diode that ensures reverse blocking protection in case of input voltage loss. The voltage difference between VIN and VSYS, denoted as VIN – VSYS, is continuously monitored. When VIN – VSYS < 25 mV, the device shuts off the power switch. This action prevents any current from flowing back to the source and effectively safeguards the source during a short circuit event.

Figure 8. Reverse blocking protection circuit (LS0502SCD33 as an example)



Linear Charge Circuit Diagram (M3 in Figure 3)

LS0502SCD33 or LS0502SCD33S works as a powerful linear charger capable of charging the supercapacitor at fast speeds, up to 350 mA, while ensuring safety. This functionality includes trickle charge (TC), constant-current (CC), and constant-voltage (CV) charge. When dealing with deeply discharged capacitors, they can utilize TC charge to precondition the capacitor using a low current level, typically half of the CC current.

Once the capacitor's voltage (VCAP) rises above 1.08 V, the device initiates CC charge mode, setting the charging current through an external resistor on the I_{CHG} pin: $R_{ICHG} = (K_{ICHG})/(I_{ICHG}) = (3.6\ A*k\Omega)/(I_{ILIM})$. This results in a linear increase in voltage during charging. The charging process progresses until the supercapacitor reaches a target voltage, which can be programmed using the VCAP feedback circuit: VCAP = [(RCFB_Top + RCFB_Bot)*1.1V]/(RCFB_Bot). The constant voltage loop comes into action at this point, accurately controlling the supercapacitor's charge level to prevent overcharging. Charging is terminated and changed to End-of-Charge (EOC) state once the CFB voltage is above 1.1 V.

Figure 9. Charge mode-TV->CC->CV->EOC

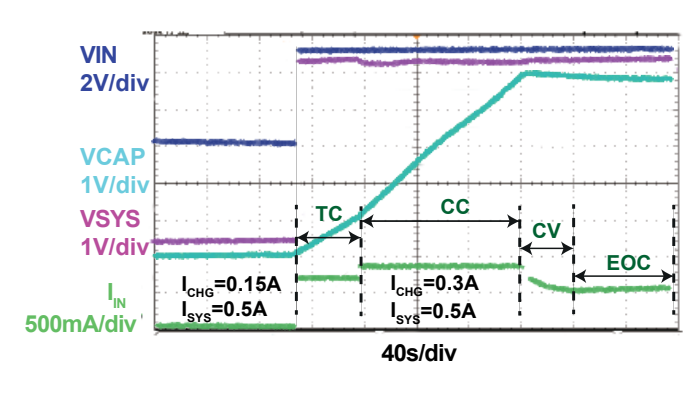
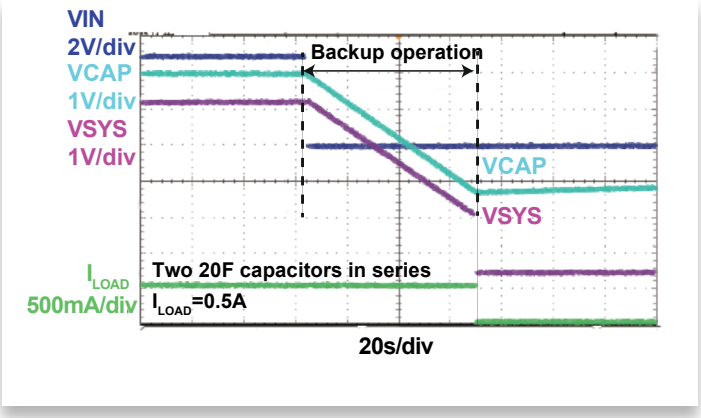


Figure 10. Discharge mode-supercapacitors backup for system



Moreover, the charging devices also function as power path control switches. In the case of input power loss, switch M3 can be turned on without interruption to provide power to system rail with low resistance path up to 2 A current in backup mode. During backup mode, the quiescent current draw from the supercapacitor is impressively low at just 2 µA, ensuring an exceptionally long standby time for the system, even with a low-capacitance supercapacitor.

Operation Modes: Standby Mode, Charge Mode, Discharge Mode and UVLO Mode

The system should have four modes: standby mode, charge mode, discharge mode, and UVLO mode, as shown in Figure 11 and 12.

Figure 11. State diagram (under charge mode, standby mode, discharge mode, UVLO mode)

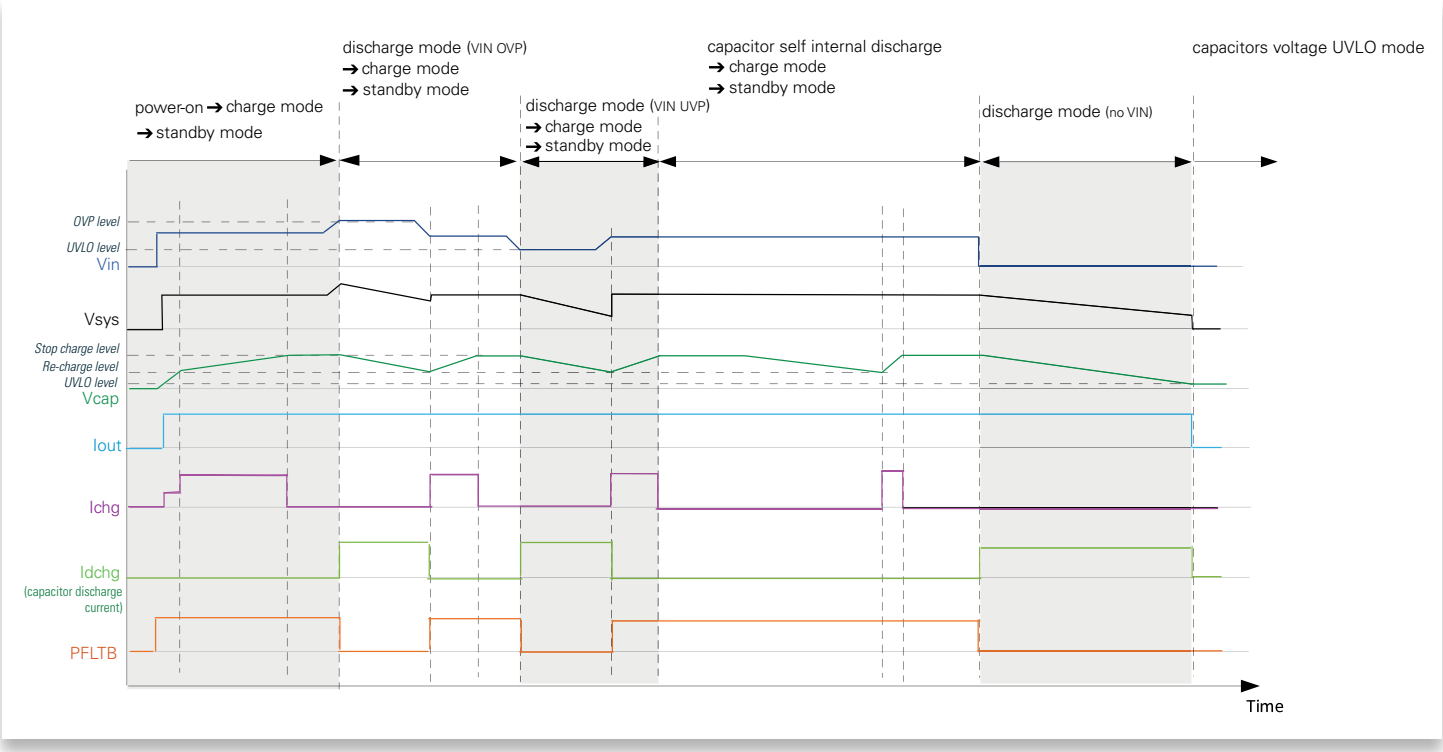
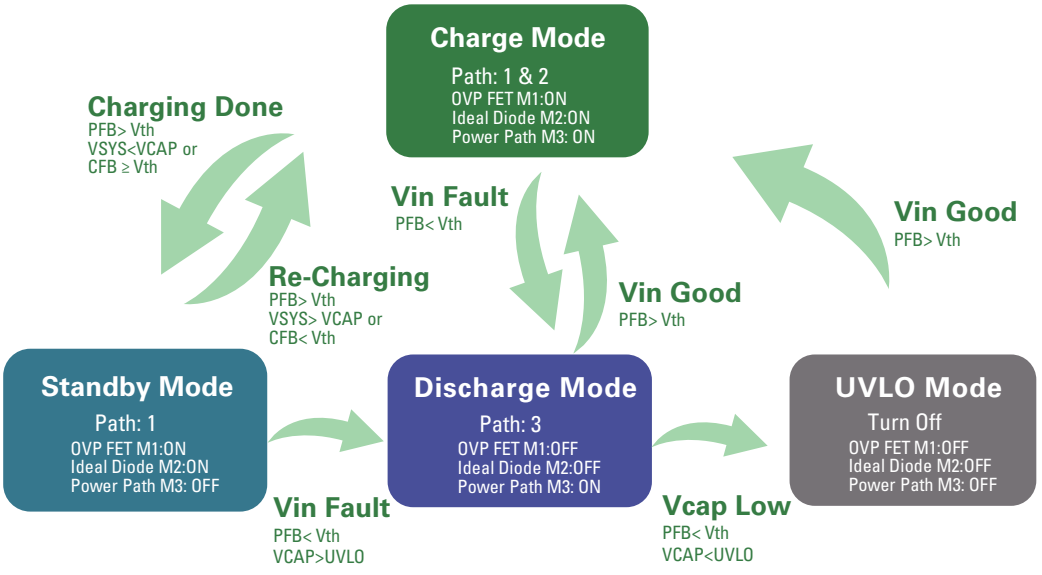


Figure 12. Operation flow diagram



Standby Mode

- When VCAP > VSYS, VIN is still available, and PFB is higher than the threshold voltage.
- Or when VCAP reaches the setting point by CFB, VIN is still available and PFB higher than the threshold.
- Or when any of the two supercapacitor voltages reaches the internal protection point and VIN is still available.

In standby mode, M3 FET should be kept OFF. The M3 body diode needs to be switched according to VSYS-VCAP voltage.

Charge Mode

When VSYS > VCAP, VIN is available and healthy; VCAP is below the setting point by CFB. Both supercapacitors are below the overvoltage protection point. In this state, turn off M3 with the current limit set by ICHG.

Two essential features that require evaluation are:

- Input DPPM (Dynamic Power Path Management): If the input voltage drops and the PFB voltage approaches the set point, it becomes necessary to fold back the charge current. This action helps limit the current drain from a weak input source.
- Soft charging ending: As VCAP is in a charged state, and the CFB voltage gets close to the set point, it is crucial to fold back the charge current. This approach prevents any potential oscillation between charge and standby modes caused by voltage drops on impedance in series with the capacitor

Discharge Mode

- If the PFB voltage falls below the threshold, it indicates the input power source is no longer available. Then the OVP FET (M1) is turned off, and the idle diode should be turned off too. The Power Path Control FET M3 is turned on, connecting VCAP to VSYS. It is essential to prevent a huge inrush current to enable a smooth transition from charge mode or standby mode to discharge mode. During this transition, it ensures the VSYS does not drop too much, as this could cause the downstream system to shut down.
- In discharge mode, all the bias current is supplied by VCAP. To extend operating time, the quiescent current needs to be below 2 uA in this case. The circuits that need to be alive are:
  - M3 over current detection circuit
  - UVLO detection circuit for VCAP

UVLO Mode

- Suppose the system operates on the supercapacitor for an extended period without recharging. In that case, the voltage of VCAP will gradually decrease, reaching a point where it can no longer sustain the entire system's function. When VCAP drops too low (less than 1.65 V), the system will enter the Under-Voltage Lockout (UVLO) mode. All circuit is shut down in this mode to preserve the system's integrity. The UVLO mode can only be cleared if VIN (input voltage) is supplied to the system.

Active Voltage Balancing (LS0502CD33, dual channel solution only)

While supercapacitors are connected in series to achieve higher voltages, voltage balancing becomes a critical issue. This is because individual devices can have capacitance variations of up to ±20 %, which can result in an overall variation of up to 40 % from one capacitor to another. The higher capacitance devices will experience greater voltage stress, which can lead to reduced operating lifetimes or even damage them. To address this issue, both passive and active approaches are used for cell balancing.

Passive voltage balancing involves using voltage-dividing resistors in parallel with each supercapacitor to balance the voltage (see Figure 13). This method is simple and cost-effective but results in power losses within the circuit. It is generally recommended for applications where supercapacitors are infrequently charged and discharged due to their limited effectiveness. For instance, using R_{BAL}=1 kΩ, the power consumption through resistances is 3.5 mW when 2.65 V is applied to the supercapacitor.

Figure 13. Passive voltage balancing circuit

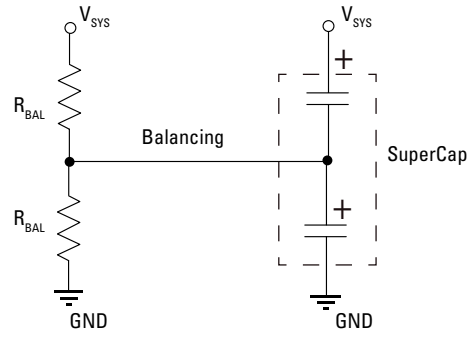
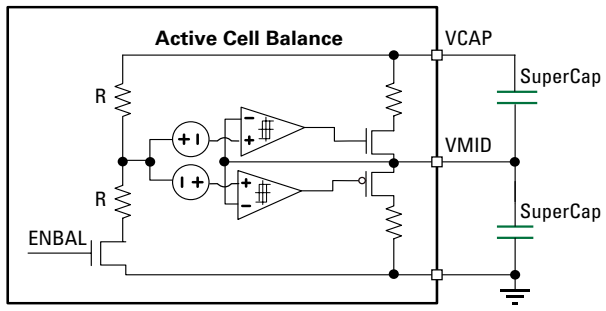


Figure 14. Active voltage balancing circuit



On the other hand, active voltage balancing circuits actively control the voltages at the nodes of the series-connected devices, ensuring they are equal to a fixed reference voltage. LS0502SCD33 also integrates active voltage balancing (see Figure 14), with the VMID pin connected to the center point of the two capacitors and the protection circuit.

During charging mode, the voltage between the two stacked capacitors (VMID pin) is compared with half of the total capacitor voltage. Current is diverted to maintain these two voltages close to each other, and the circuit continuously monitors the voltage for each capacitor. If any capacitor voltage reaches 2.65V during charging, the charging process is halted, and recovery charging is enabled for the capacitor under 2.65 V with cell balancing. This is achieved by reducing the charge current by about 3 mA maximum to balance the two-connected supercapacitors. to balance the two-connected supercapacitors. Similarly, during discharge mode, discharging is stopped to protect the capacitors if any capacitor voltages drop below ground.

While active voltage balancing is more complex, it offers higher efficiency and accuracy in maintaining balanced voltages across the supercapacitors. This results in longer lifespans and improved performance for the overall system.

Table 2. Comparison of passive voltage balance and active voltage balance

Feature	Passive Voltage Balance	Active Voltage Balance
Area	small	large
Power conosumption	low (1 mΩ)~high (1 kΩ)	middle
Operation speed	slow	fast
Control of charge voltage	impossible	possible
Voltage balancing effectiveness	low	high
Cost	low	high

Input Current Limit and Short Circuit Protection

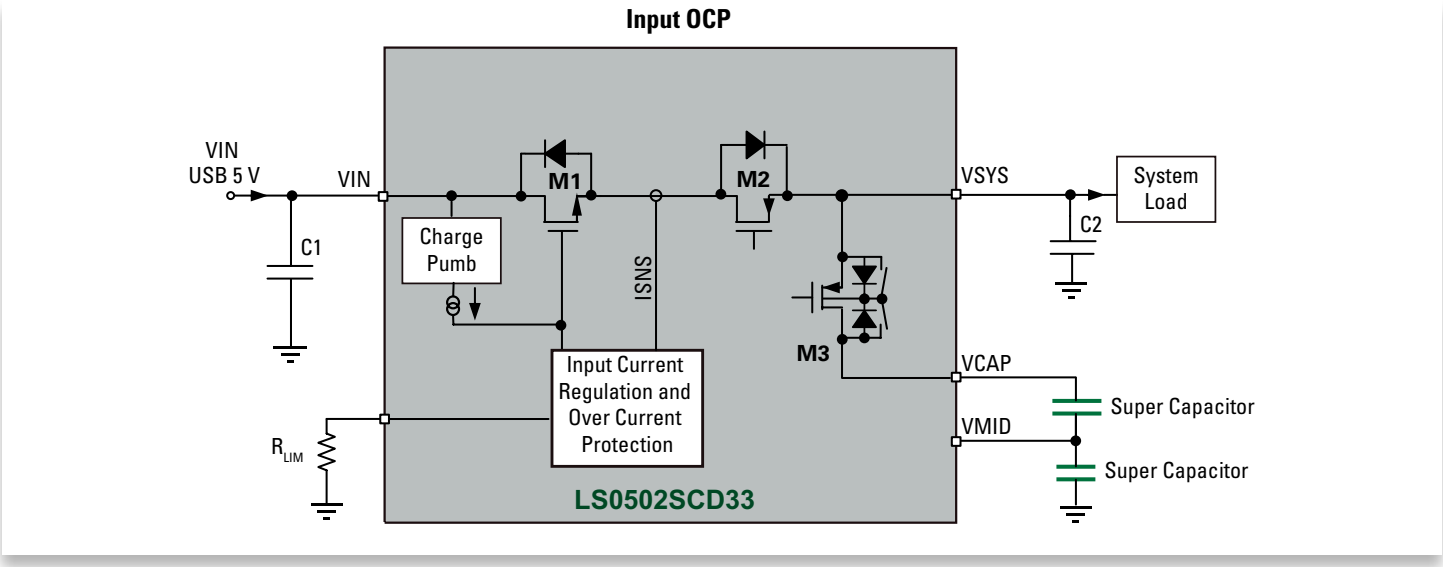
For current-limited adaptors or power sources, users can program the input current limit level in charger mode, preventing the load current from overloading the power source. LS0502SCD33 or LS0502SCD33S allows setting the input current limit through an external resistor, R_{ILIMT}, connected between I_{LIMT} and GND. If an overload occurs, the internal circuitry restricts the input current based on the value of R_{ILIM} and pulls the PFLTB pin LOW to indicate a fault condition. The current limit resistor R_{ILIMT} is determined using the equation: $R_{ILIM} = K_{ILIM}/I_{ILIM} = 30\ A*k\Omega/I_{ILIM}$. The common current limit threshold settings are provided in the table below.

Additionally, LS0502SCD33 or LS0502SCD33S can integrate a fast-trip comparator to promptly turn off the power switch when the output voltage is shorted to ground. In charge mode, the device operates in hiccup mode for short circuit protection. When a short circuit fault is detected, the power switch is turned off, and PFLTB transitions from high to low, as depicted in Figure 7. After a predetermined duration, the device attempts to restart to soft-start the power switch. If the overload condition has been removed, the power switch will turn on and function normally. Otherwise, the device will encounter another over-current event, leading to the power switch being shut off again, repeating the cycle.

Table 3. Input current Limit setting by an external resistor R_{ILIM}

R_{ILIM} (kΩ)	60	30	15	0
Current Limit I_{ILIM} (A)	0.5	1	2	2.7

Figure 15. Circuit of charge mode VSYS short protection (LS0502SCD33 as an example)



During the hiccup cycle, the excess heat due to overload lasts for only a short duration, leading to significantly lower junction temperatures for the power devices. For example, with 5 Vin, hiccup mode current of 2.5 A, hiccup mode on time of 160 µs, and off time of 8 ms, the average power loss is only: 5 V*2.2 A*(160 µs/8 ms) = 0.22 W. This mechanism efficiently manages overload, ensuring the system's protection and minimizing heat-related issues during fault conditions.

Figure 16. Waveform of charge mode VSYS short protection under 4 ms/div (cycle time is 8 ms)

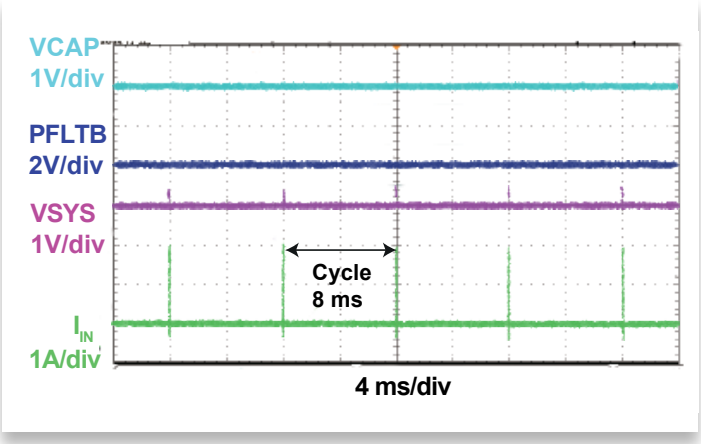
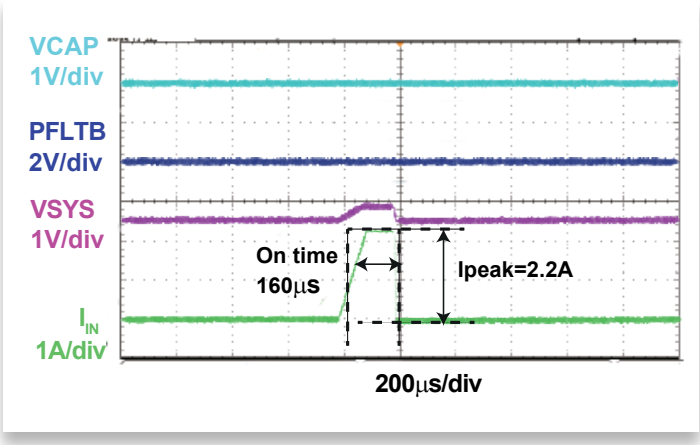


Figure 17. Waveform of charge mode VSYS short protection under 200 µs/div (the zoom-in look of figure 16)



Summary

Supercapacitors have shown great potential for applications in harsh operating environments, requiring high storage energy, instant power capability, long standby time, and maintenance-free deployment. While engineers can implement supercapacitor charging circuits using conventional switched converters, maximizing supercapacitor efficiency and lifespan necessitates a reliable and flexible power management IC with monitoring and protection features.

The LS0502SCD33 or LS0502SCD33S offers fully integrated power management solutions tailored for systems with supercapacitor backup power applications. They provide programmable overcurrent protection, input power failure detection, and configurable supercapacitor charge voltage settings. Additionally, they include integrated input power source overvoltage protection, safeguarding the system from input surges. Furthermore, their input power source reverse blocking circuit ensure the supercapacitors are protected from discharging through the input terminal.

During backup mode, when the system draws power from the supercapacitor, LS0502SCD33 or LS0502SCD33S only draws 2 µA current from the supercapacitor. This feature ensures prolonged standby time for systems requiring continuous operation for days or weeks, utilizing low-power circuitry like real-time clocks or monitoring functions.

They represent remarkable advancement in available supercapacitor charge ICs, enabling engineers to enhance energy-harvesting designs by incorporating supercapacitors. Their comprehensive features and efficiency make them exceptional choice for engineers seeking reliable and effective power management solutions.

For more information about LS0502SCD33 and LS0502SCD33S, please use the following links on Littelfuse website

Product series page

LS0502SCD33: https://www.littelfuse.com/products/protection-ic/efuse/ls0502scd33.aspx

LS0502SCD33S: https://www.littelfuse.com/products/protection-ic/efuse/ls0502scd33s.aspx

Evaluation board

Please contact sales@littelfuse.com for information about the LS0502SCD33 or LS0502SCD33S evaluation board.

Figure 18. LS0502SCD33 evaluation board.