

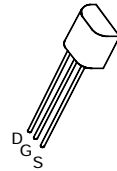
# N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

## ZVNL110A

ISSUE 2 – MARCH 94

### FEATURES

- \* 100 Volt  $V_{DS}$
- \*  $R_{DS(on)}=3\Omega$
- \* Low threshold voltage



E-Line  
TO92 Compatible

### ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	100	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	$I_D$	320	mA
Pulsed Drain Current	$I_{DM}$	6	A
Gate Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation at $T_{amb}=25^{\circ}C$	$P_{tot}$	700	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	100		V	$I_D=1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.75	1.5	V	$I_D=1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	$I_{GSS}$		100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	$I_{DSS}$		10 500	$\mu A$ $\mu A$	$V_{DS}=100V, V_{GS}=0$ $V_{DS}=80V, V_{GS}=0V, T=125^{\circ}C$ (2)
On-State Drain Current(1)	$I_{D(on)}$	750		mA	$V_{DS}=25V, V_{GS}=5V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		4.5 3.0	$\Omega$ $\Omega$	$V_{GS}=5V, I_D=250mA$ $V_{GS}=10V, I_D=500mA$
Forward Transconductance (1)(2)	$g_{fs}$	225		mS	$V_{DS}=25V, I_D=500mA$
Input Capacitance (2)	$C_{iss}$		75	pF	$V_{DS}=25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	$C_{oss}$		25	pF	
Reverse Transfer Capacitance (2)	$C_{rss}$		8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	$V_{DD}=25V, V_{GS}=10V, I_D=1A$
Rise Time (2)(3)	$t_r$		12	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		15	ns	
Fall Time (2)(3)	$t_f$		13	ns	

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