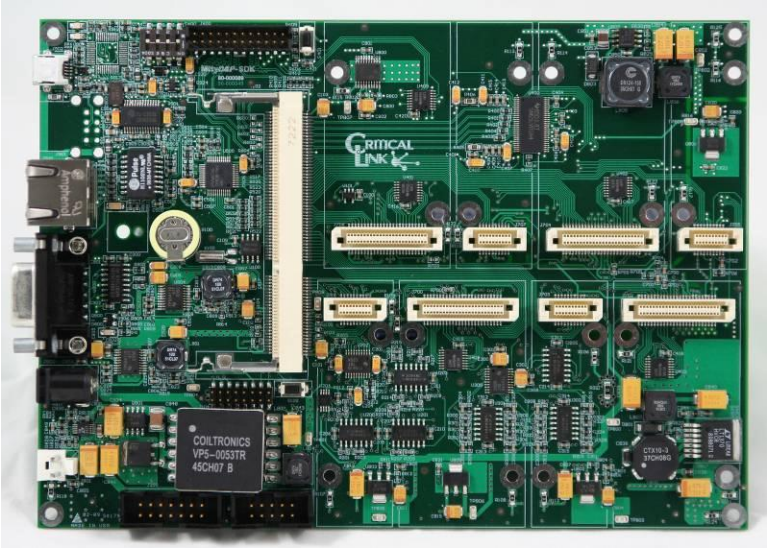
FEATURES

- Standard MityDSP SO-DIMM-144 Interface
- RS-232 Serial Interface
- USB Interface
  - 1.2/2.0 Compatible
  - 6 MBit Link Speed
  - Windows Drivers Available
- 10/100 MBit Ethernet Interface
- 5 High Speed LVDS Pairs
  - Supports Quarter VGA Interface
- 8 On-Board Digital to Analog Converters
  - 12 Bit resolution
  - 1 µs settling time
- 8 On-Board Analog to Digital Converters
  - 12 Bit resolution
  - 200 Ksps sample rate
- On-board Real Time Clock
- Four MDK-4 Daughter Card Expansion Slots
- Four MDK-8 Daughter Card Expansion Slots

APPLICATIONS

- MityDSP Evaluation
- Embedded Instrumentation
- Rapid Prototyping
- Control Processing
- Remote Sensing
- Embedded Signal Processing



DESCRIPTION

The MityDSP Development Kit Motherboard (MDK-MB), Revision B, provides a low-cost target platform for integration and development using the MityDSP based family of Processor Cards. The MDK-MB is fully compatible with MityDSP and MityDSP-XM processor cards with Bank 7 configured in LVDS mode. The MDK-MB includes on board RS-232, 10/100 MBit Ethernet and Universal Serial Bus (USB) communications interfaces. For basic data acquisition and control, an 8 channel 12-bit DAC and an 8 channel 12-bit ADC is included. For display, an LVDS link connection to an off-board quarter VGA (QGVA) display controller with backlight driver is provided.

In addition to the on-board I/O interfaces, the MDK-MB provides interfaces for four MityDSP Development Kit (MDK) MDK-8 and four MDK-4 form factor daughter card sites for system expansion. The daughter card sites are laid-out to also allow the use of MDK-12, MDK-16, and MDK-24 size daughter cards by combining card slots as described in the Daughter Card Configuration section, below. The MDK daughter cards allow customization of the system card based on the application. Users may select from several off-the-shelf cards available from Critical Link or design their own based on their specific requirements.

The MDK-Pro-MB includes on board voltage regulation for providing power digital and analog circuits. The card requires a power supply capable of providing a nominal +9 to +18 Volts DC. Input power can be supplied via the 2-pin 0.156" Molex header, or a standard barrel-style power jack.

A block diagram of the MDK-MB is illustrated in Figure 1. All available FPGA I/O lines and the two 6711 McBSP ports are either used directly by the MDK-MB or are routed to the MDK daughter card sites. Control of the on-board interface hardware and connected daughter cards require proper configuration of the MityDSP FPGA and DSP. While not required, it is strongly recommended that the MityDSP software and firmware development kit and supplied API be used to manage these interfaces.

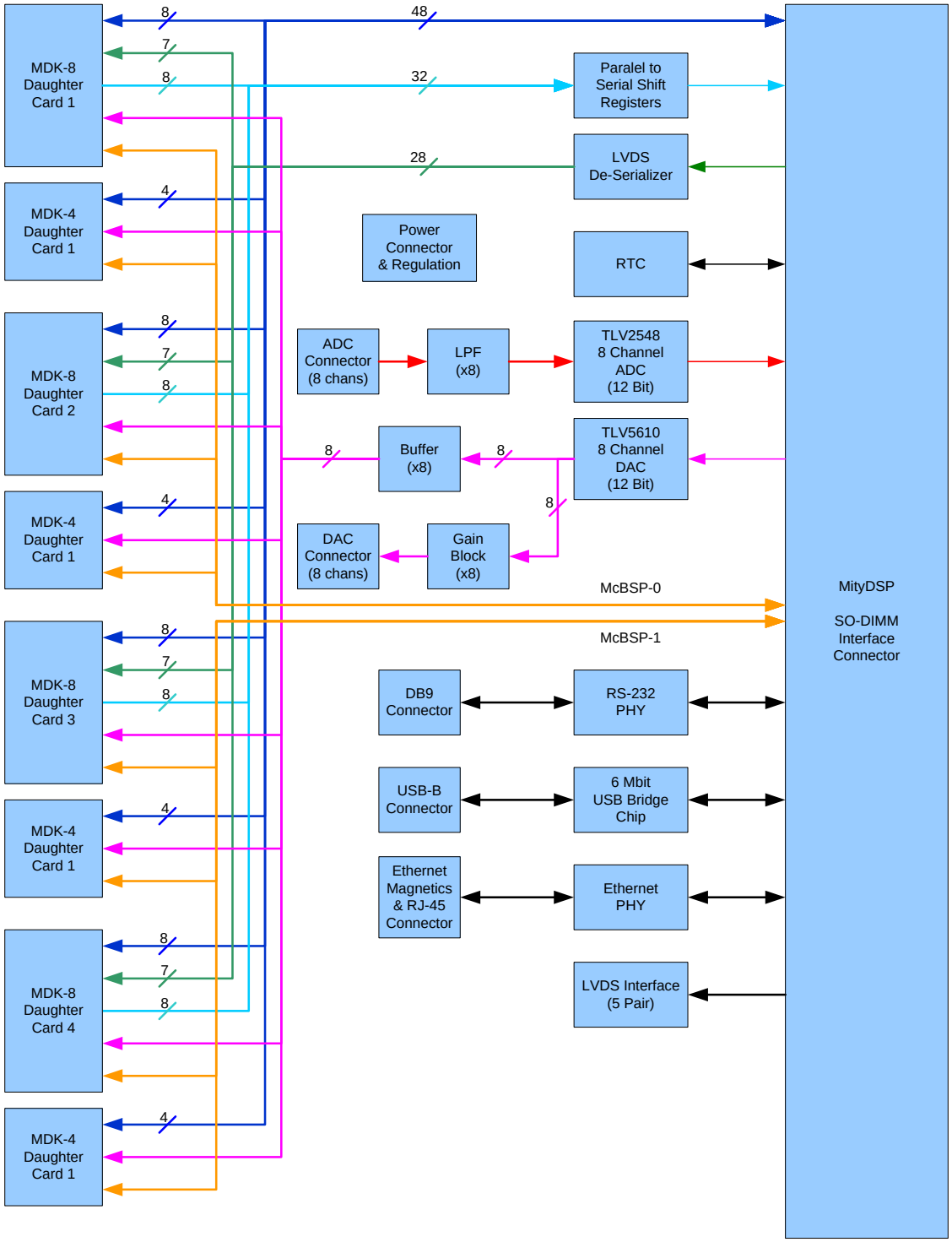


Figure 1: MityDSP Development Kit Block Diagram

RS-232 Interface Description
The on-board RS-232 level driver and DB-9 connector provides standard serial interface at data rates up to 115,200 baud. The serial interface is routed to the primary MityDSP serial bootloading port in order to allow remote code download and FLASH upgrades on an attached MityDSP from this connector.

USB Interface Description
The on-board USB interface leverages an asynchronous serial to USB 2.0 compliant bridge chip that supports data rates up to 6 Mbits per second. Drivers for the USB interface are provided with the MityDSP software development kit and are compatible with Windows XP, 2000, and Vista. The USB serial interface is routed to the alternate MityDSP serial bootloading port in order to allow remote code download and FLASH upgrades on an attached MityDSP from this connector.

Ethernet Interface Description
The on-board Ethernet interface features a network PHY capable of running at 10/100 Mbit including link auto-negotiation and MII/MDIO capability. An industry standard RJ-45 connector is provided for external connection. Use of the Ethernet interface requires an Ethernet Media Access Controller (MAC) implementation in the MityDSP FPGA. The MityDSP hardware and software development kit includes a full tested Ethernet MAC as well as an implementation of the LwIP TCP/IP stack, providing a full Ethernet capable platform ready for integration. This Ethernet interface may be used to perform remote code download and FLASH upgrades on an attached MityDSP.

LVDS Interface Description
The MDK-MB provides a flat-ribbon cable low profile interface for five Low Voltage Differential Signaling (LVDS) pairs. The interface design is intended to support high speed off board interconnects. In addition to custom user interfacing, the pairs may be used to interface to a Quarter VGA LCD screen using the MityDSP hardware and software development kit LCD interface libraries and an appropriate daughterboard interface. Off-the-shelf display solutions for QVGA interfaces are provided by Critical Link.

DAC Description
The MDK-MB provides an on-board 8 channel 12-bit digital to analog converter to the MityDSP's TI C6711 DSP via McBSP port 1. The DAC part is the TLV5610 from Texas Instruments® / Burr Brown® and is capable of output settling times of 1 µs.

The eight channels are routed to the external DAC connector J200, a standard dual-row, 14-pin, 0.1" pitch shrouded header. All channels provide a voltage output range of 0 to 10 Volts with respect to AGND, and are buffered to provide an output impedance of less than 300 ohms.

The eight channels are also independently buffered and routed (1 each) to the four MDK-8 and the four MDK-4 daughter card slots, and provide an output range of 0 to 4.096 Volts. Note: Use of a daughter card that requires the use an associated DAC line implies that the corresponding pin on the external DAC connector should not be used. Please refer to the data sheet for a specific daughter card in order to determine if the DAC channel is required.

For details regarding the signal interface to the MityDSP McBSP port, please refer to the MDK-MB reference schematic. The MityDSP software development kit includes an API for interfacing to the TLV5610.

ADC Description

The MDK-MB provides an on-board 8 channel 12-bit analog to digital converter to the MityDSP's TI C6711 DSP via McBSP port 0. The ADC component is the TLV2548 from Texas Instruments® / Burr Brown® and is capable of sampling at rates up to 200 Ksps, aggregate.

The eight input channels enter the board via a standard dual-row, 10-pin, 0.1" pitch shrouded header, J301. All input channels have an input range of 0 to 10 Volts with respect to AGND, and have an input impedance of 10k ohms. The signals are unity-gain buffered, and then low-pass filtered using a simple R/C network having a –3dB corner frequency of 48 kHz.

For details regarding the signal interface to the MityDSP McBSP port, please refer to the MDK-MB reference schematic. The MityDSP software development kit includes an API for interfacing to the TLV2548.

Real Time Clock Description

The MDK-MB provides a real-time clock using an I2C device with part number M41T81SM6F. Use of the RTC requires an implementation of an I2C driver interface within the FPGA of the MityDSP. The MityDSP software development kit includes an API for interfacing to the M41T81SM6F.

For details regarding the signal interface to the MityDSP I/O pins, please refer to the MDK-MB reference schematic.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	19 V
Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range	0 to 55C
Humidity	0 to 95% Non-condensing
Vibration, Z-Axis	TBS
Vibration, X/Y-Axis	TBS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Power Dissipation					
V_S	Supply Voltage.		12	9 / 18	Volts (Min/Max)
I_S	Supply Current.		0.33[1]	1.0	Amps (Max)
On-Board Analog To Digital Converter					
BW_{ADC}	3 DB Bandwidth Analog to Digital Converter	R/C filtering	48	-	KHz
$V_{Min,ADC}$	Minimum Analog Input Voltage		0	TBD	Volts
$V_{Max,ADC}$	Maximum Analog Input Voltage		10	TBD	Volts
Fs_{ADC}	Maximum Sample Rate, ADC			TBD	KHz
$R_{IN,\ ADC\text{-}Ext}t$	Input Impedance		10	8	KOhms (Min)
On-Board Digital To Analog Converter					
$V_{Min,DAC\text{-}Ext}$	Minimum Analog Input Voltage, External DAC connection.		0	-0.2	Volts
$V_{Max,DAC\text{-}Ext}$	Maximum Analog Input voltage External DAC connection.		10	10.2	Volts
$V_{Min,DAC\text{-}DBC}$	Minimum Analog Input Voltage, MDK-4/8 Daughter Board DAC Interface.		0	-0.2	Volts
$V_{Max,DAC\text{-}DBC}$	Maximum Analog Input Voltage, MDK-4/8 Daughter Board DAC Interface.		4.096	4.3	Volts
Fs_{DAC}	Maximum Output Sample Rate, DAC		2	200	KHz
$R_{out\ DAC\text{-}Ext}$	Output Impedance		200	300	Ohms (Max)
MDK-8 Digital I/O					
$F_{clk,din}$	Clock Frequency, Digital Inputs		25	25	MHz
$T_{update,din}$	Update Period, Digital Inputs		1680	1680	ns
$F_{clk,dout}$	Clock Frequency, Digital Output LVDS clk entering deserializer		50	20 / 68	MHz (Min/Max)
$T_{update,dout}$	Update Period, Digital Outputs		20	14.7 / 50	ns (Min/Max)
Notes:	1. Power Supply load is dependent on Daughter Card configuration and utilization.				

DAUGHTER CARD CONFIGURATION

The MDK-MB and daughter card system provides a high level of flexibility in configuration in order to maximize the use of the available MityDSP expansion pins. The daughter cards used in the MDK system are sized according to their complexity and number of required I/O pins to the MityDSP. There are several possible form factors: MDK-4, MDK-8, MDK-12, MDK-16, MDK-24, and MDK-48. The primary form factors, however, are the MDK-4 and MDK-8 configurations. All of the other factors listed are simply a combination of these card sizes.

Figure 2 provides a top view of the MDK-MB circuit card and its corresponding interface connectors. In the figure, the daughter card sites are located on the right hand side of the board. The basic MDK-4 and MDK-8 card connectors are divided evenly into the top half of the card and the bottom half of the card. While this section illustrates configurations for the bottom half of the card, please note that the top half provides similar connectivity.

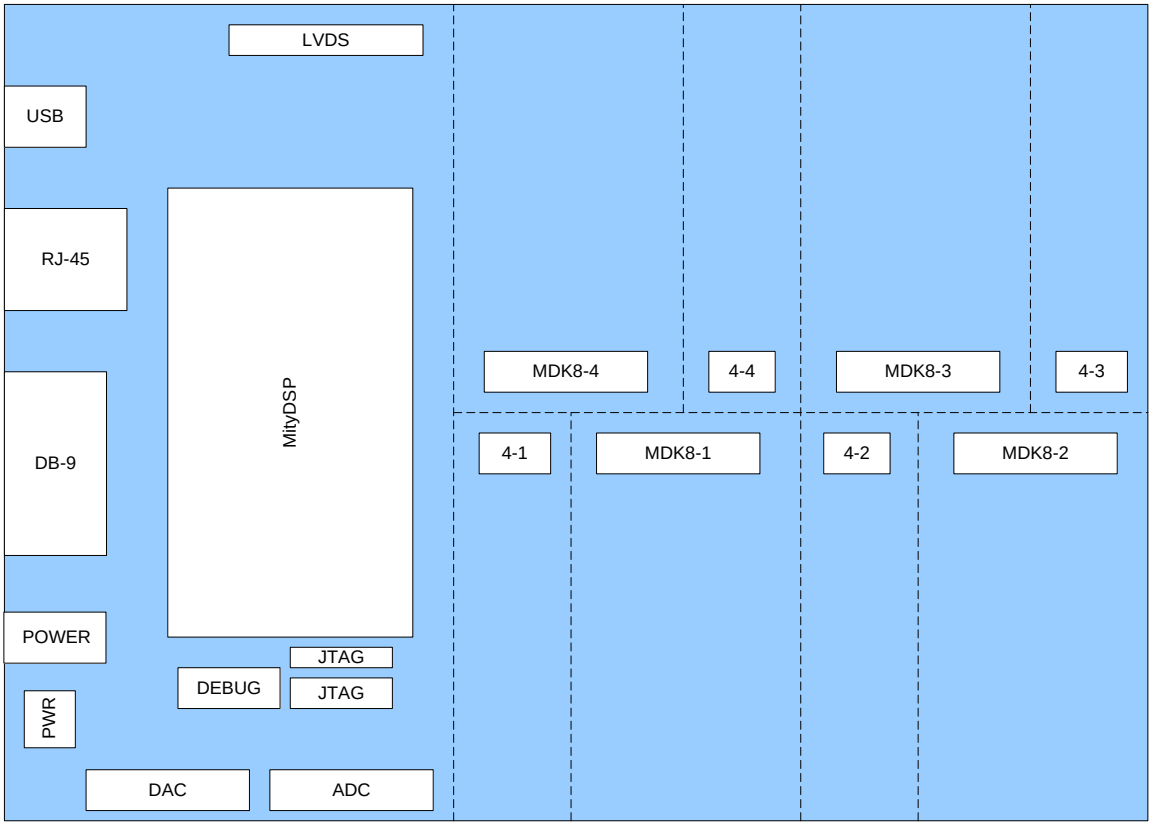


Figure 2: MDK-MB Connector Locations, Top View

Figure 3 illustrates the bottom half of the MDK-MB daughter card expansion area using two each of the MDK-4 and MDK-8 form factor daughter cards. In this configuration, the cards are simply plugged into their corresponding connectors on the board.

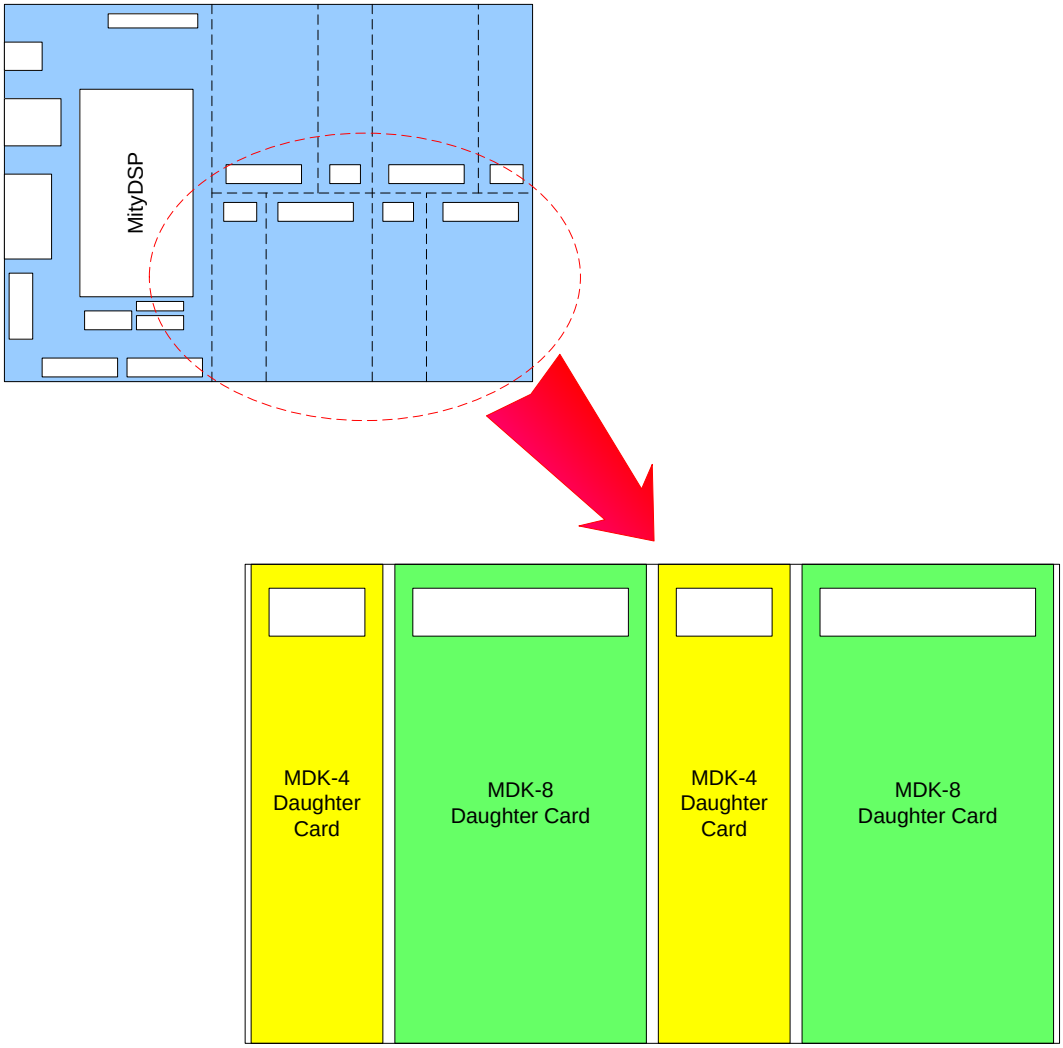


Figure 3: Daughter Card Configuration, 2 MDK-4 and 2 MDK-8 Cards (Top View)

Figure 4 illustrates the use of MDK-12 form factor daughter cards, which occupy one each of the MDK-4 and MDK-8 slot connectors. As is shown in Figure 5, the MDK-12 cards may be mixed and matched with MDK-4 or MDK-8 cards in an MDK-MB configuration. Card slots may be left empty.

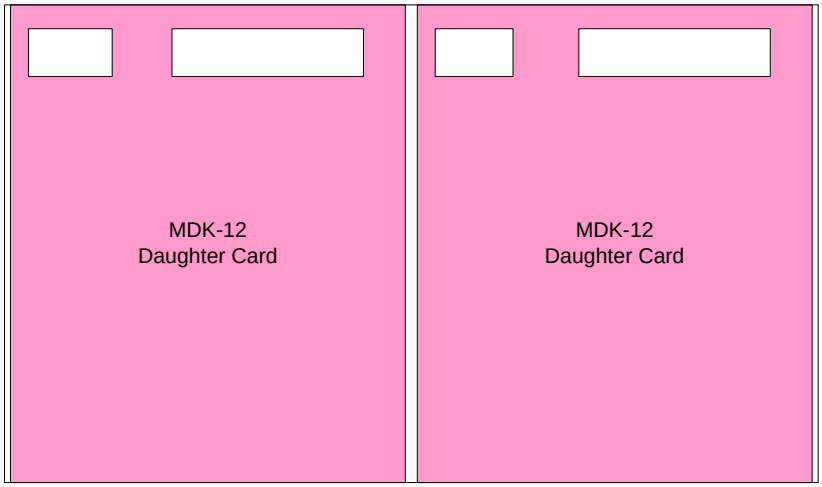


Figure 4: Daughter Card Configuration, 2 MDK-12 Cards (Top View)

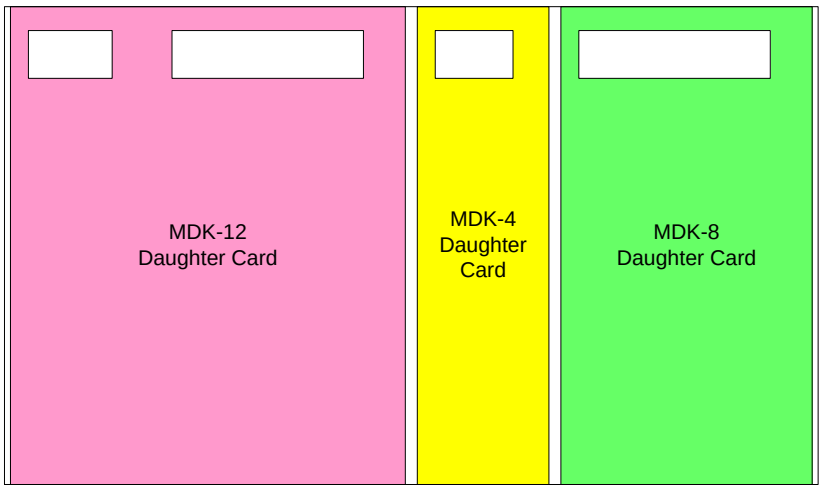


Figure 5: Daughter Card Configuration, 1 each MDK-12, MDK-4, and MDK-8 (Top View)

Use of an MDK-16 Daughter Card requires two MDK-4 slots and an MDK-8 slot as shown in Figure 6.

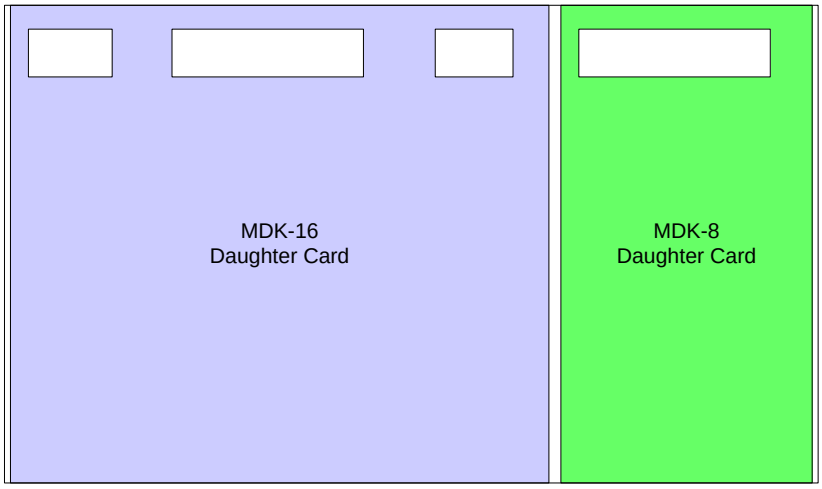


Figure 6: Daughter Card Configuration, MDK-16 and MDK-8 (Top View)

The MD-24 uses two each of the MDK-4 and MDK-8 slots as shown in Figure 7. Similarly (and not shown), an MDK-48 card would use all available slots on the MDK-MB. MDK-48 cards are typically full custom designs.

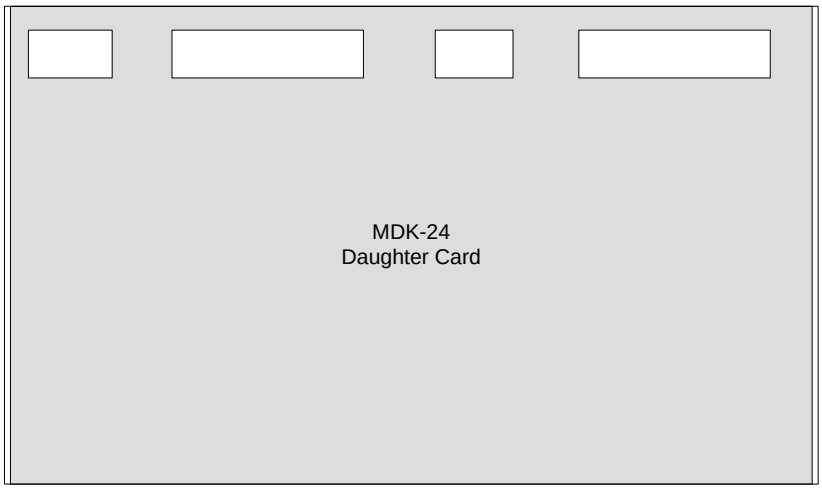


Figure 7: Daughter Card Configuration MDK-24 (Top View)

ELECTRICAL INTERFACE DESCRIPTION

MityDSP JTAG Interface

The MDK-MB provides a Critical Link standard combined interface for DSP and FPGA JTAG access. The connector is a 16-pin, dual-row 2 mm header, with pinout described below in Table 1.

Table 1: JTAG Connector Pin-Out

Pin	Signal	Signal	Pin
1	DSP_EMU0	DSP_TMS	2
3	DSP_EMU1	DSP_TDI	4
5	3.3V	DSP_TDO	6
7	GND	DSP_TCK	8
9	GND	DSP_TRST#	10
11	FPGA_TDI	FPGA_TMS	12
13	FPGA_TCK	FPGA_TDO	14
15	GND	2.5V	16

Input Power

The MDK-MB power interface, J800 or J801, requires a single +9 to +18 Volt power supply. J800 is a 2.1mm-ID, 5.5mm-OD barrel-style power jack, center-positive. J801 is a standard 2-pin, 0.156" pitch Molex locking header. The Pin-out for the power interfaces is included in Table 2.

Table 2: Input Power Interface Pin Description

Signal	J800 Position	J801 Position
+9 to +18 Volts	Center-pin	1
GND	Outer-ring	2

Analog I/O Connectors

The MDK-MB provides two double-row shrouded connectors for the on-board DAC circuit outputs and the on board ADC connectors. Table 3 defines the DAC external interface connectors. A cable using AMP® connector 1658621-2 (or equivalent) should be used. All channels provide a voltage output range of 0 to 10 Volts with respect to AGND, and are buffered to provide an output impedance of less than 300 ohms. Note that all DAC outputs are also shared with the MDK daughter card slots. MDK cards that require use of the DACs preclude the use of the external interface DAC channel.

Table 3: J200 On-Board DAC External Interface Connector

Pin	Signal	Shared Slot
1	AGND	N/A
2	AGND	N/A
3	AGND	N/A
4	DAC_1	MDK8-1
5	DAC_2	MDK8-2
6	DAC_3	MDK8-3
7	DAC_4	MDK8-4
8	DAC_5	MDK4-1
9	DAC_6	MDK4-2
10	DAC_7	MDK4-3
11	DAC_8	MDK4-4
12	AGND	N/A
13	AGND	N/A
14	AGND	N/A

Table 4 defines the ADC external interface connectors. A cable using AMP® connector 1658621-1 (or equivalent) should be used. All input channels have an input range of 0 to 10 Volts with respect to AGND, and have an input impedance of 10k ohms.

Table 4: J301 On-Board ADC External Interface Connector

Pin	Signal
1	AGND
2	ADC_1
3	ADC_2
4	ADC_3
5	ADC_4
6	ADC_5
7	ADC_6
8	ADC_7
9	ADC_8
10	AGND

LVDS Interface

The LVDS interface connector provides up to 5 pairs of LVDS signals connected to the Spartan 3 device on a connected MityDSP. The interfaces uses a standard 2 mm 24 position male header. Table 5 defines the LVDS connector pinout. A cable using AMP® TBD connector (or equivalent) should be used. Use of the LVDS pairs as outputs will require addition of termination resistors (100 Ohm) on externally designed circuit assemblies. Use of the LVDS pairs as inputs will require population of 0603 sized termination resistors on the MDK-MB on the provided solder pads. Refer to the detailed schematic and assembly drawing for further information.

Table 5: J600 LVDS Interface Pin Description

Pin	Signal	Type	Standard	Notes
1	+5 V	-	-	500 mA Max.
2	+5 V	-	-	500 mA Max.
3	GND	-	-	
4	GND	-	-	
5	DISP_A0_P	I/O	LVDS	Display/LVDS Data channel 0
6	DISP_A0_N	I/O	LVDS	Display/LVDS Data channel 0
7	DISP_A1_P	I/O	LVDS	Display/LVDS Data channel 1
8	DISP_A1_N	I/O	LVDS	Display/LVDS Data channel 1
9	DISP_A2_P	I/O	LVDS	Display/LVDS Data channel 2
10	DISP_A2_N	I/O	LVDS	Display/LVDS Data channel 2
11	DISP_A3_P	I/O	LVDS	Display/LVDS Data channel 3
12	DISP_A3_N	I/O	LVDS	Display/LVDS Data channel 3
13	GND	-	-	
14	GND	-	-	
15	DISP_CLKIN_P	I/O	LVDS	Display/LVDS Clock (or Data)
16	DISP_CLKIN_N	I/O	LVDS	Display/LVDS Clock (or Data)
17	GND	-	-	
18	P_SW	I/O/PU	CMOS	Display Aux. I/O (push-button switch)
19	DISP_I2	I	CMOS	Display Touch-screen Input 2
20	DISP_I1	I	CMOS	Display Touch-screen Input 1
21	DISP_I0	I	CMOS	Display Touch-screen Input 0
22	DISP_O2	O	CMOS	Display Touch-screen Output 2
23	DISP_O1	O	CMOS	Display Touch-screen Output 1
24	DISP_O0	O	CMOS	Display Touch-screen Output 0

MDK-8 Daughter Card Interface

The MDK-MB provides 4 MDK-8 Daughter Card interface positions. Each position includes one 50 position dual row sockets. Mating connectors for these sockets are the Hirose FX6-50P-0.8SV plugs. Table 6 defines the signals on each pin for the cards. Table 8 provides the electrical standards for the various nets.

Table 6: Daughter Card – MDK-8 Connector Pin Assignments

Pin	Signal	Pin	Signal
A1	IO_0	B1	+5 V
A2	IO_1	B2	+5 V
A3	IO_2	B3	+3.3 V
A4	IO_3	B4	+3.3 V
A5	IO_4	B5	+12 VA
A6	IO_5	B6	GND
A7	IO_6	B7	GND
A8	IO_7	B8	GND
A9	DO_0	B9	-12 VA
A10	DO_1	B10	+15 V
A11	DO_2	B11	+15 V
A12	DO_3	B12	-15 V
A13	DO_4	B13	-15 V
A14	DO_5	B14	AGND
A15	DO_6	B15	AGND
A16	DI_0	B16	DO_CLK
A17	DI_1	B17	RSV
A18	DI_2	B18	RSV
A19	DI_3	B19	RSV
A20	DI_4	B20	RSV
A21	DI_5	B21	RSV
A22	DI_6	B22	RSV
A23	DI_7	B23	RSV
A24	ADC	B24	RSV
A25	DAC	B25	RSV

MDK-4 Daughter Card Interface

provides 4 MDK-4 Daughter Card interface positions. Each position includes one 20 position dual row socket. Mating connectors for these sockets are the Hirose FX6-20P-0.8SV plugs. Table 7 defines the signals on each pin for the cards. Table 8 provides the electrical standards for the various nets.

Table 7: Daughter Card MDK-4 Connector Assignments

Pin	Signal	Pin	Signal
A1	IO_0	B1	+5V
A2	IO_1	B2	+5V
A3	IO_2	B3	+3.3V
A4	IO_3	B4	+3.3V
A5	+15 V	B5	GND
A6	+15 V	B6	GND
A7	DAC	B7	RSV
A8	AGND	B8	RSV
A9	RSV	B9	RSV
A10	RSV	B10	RSV

Daughter Card Signal Description

Table 8: Daughter Card Signal Description

Signal	Type	Standard	Notes
IO_##	I/O	3.3V CMOS	Direct Interface to MityDSP-Pro Spartan3 FPGA.
DO_##	O	3.3V CMOS	Digital Output. Update Rate of 20 nsec. DO_CLK provides sampling clock – outputs should be sampled on rising edge.
DI_##	I	3.3V CMOS	Digital Input. Sampling interval < 2 µs.
DAC_1 DAC_2 DAC_3 DAC_4	O	0-4.096 V	12 Bit.
ADC_1 ADC_2 ADC_3 ADC_4	I	0-2 V	12 Bit. 10 Khz R/C filtering.

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

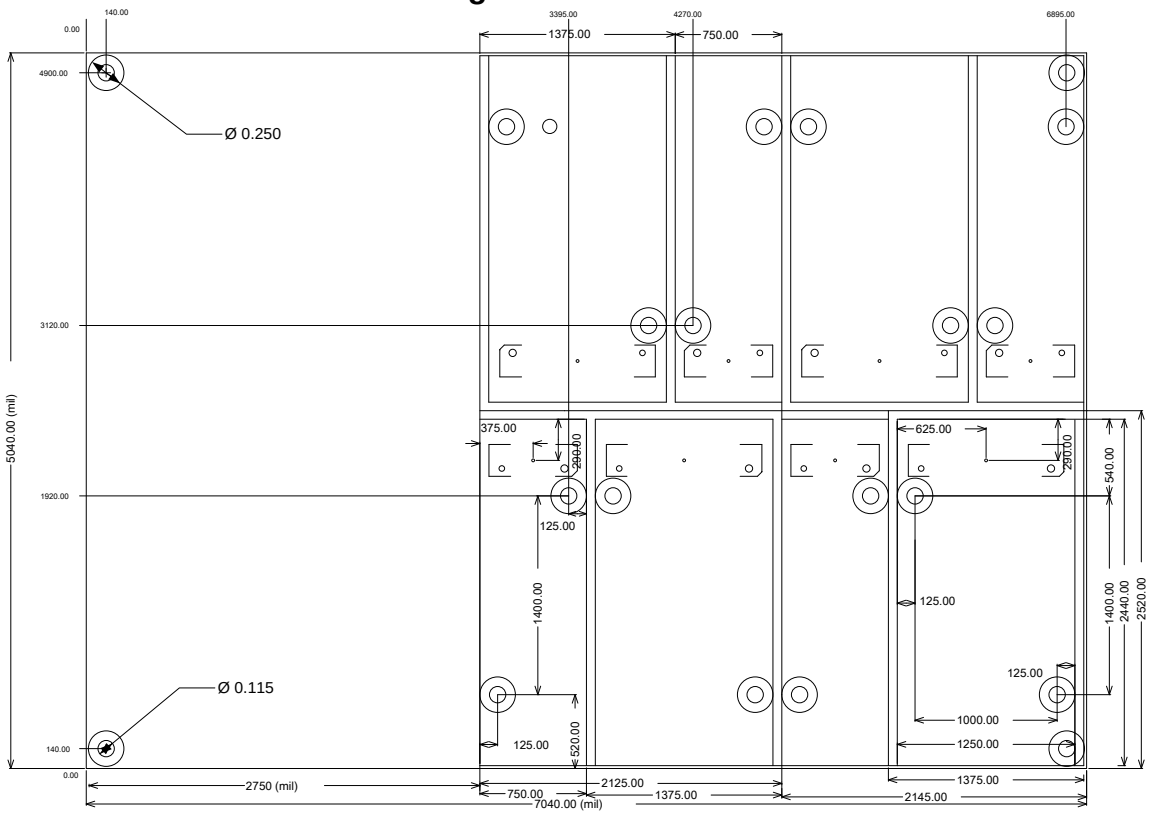


Figure 8: MDK-MB PCB Outline and Mounting Hole Locations (Top View, mils)

Daughter Card Interface / Mounting

Mechanical outlines for each of the MDK-4 and MDK-8 form factors are shown in Figure 9 and Figure 10, respectively. For larger MDK-12, MDK-16, and MDK-24 form factors, a 1/16th inch gap (62.5 mils) is required between each of the board outlines. Figure 11 illustrates an MDK-12 form factor board with the necessary spacing.

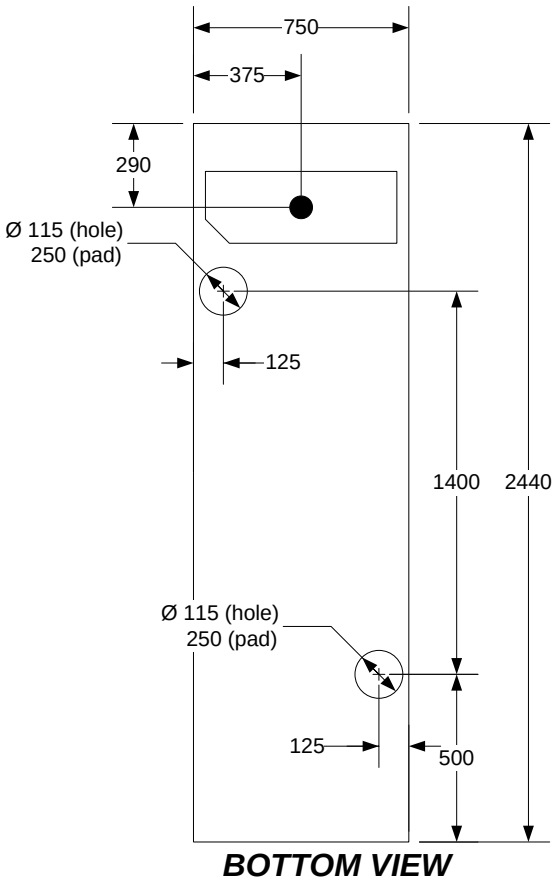


Figure 9: MDK-4 Mounting Hole, Size, and Hirose Connector location (units in mils)

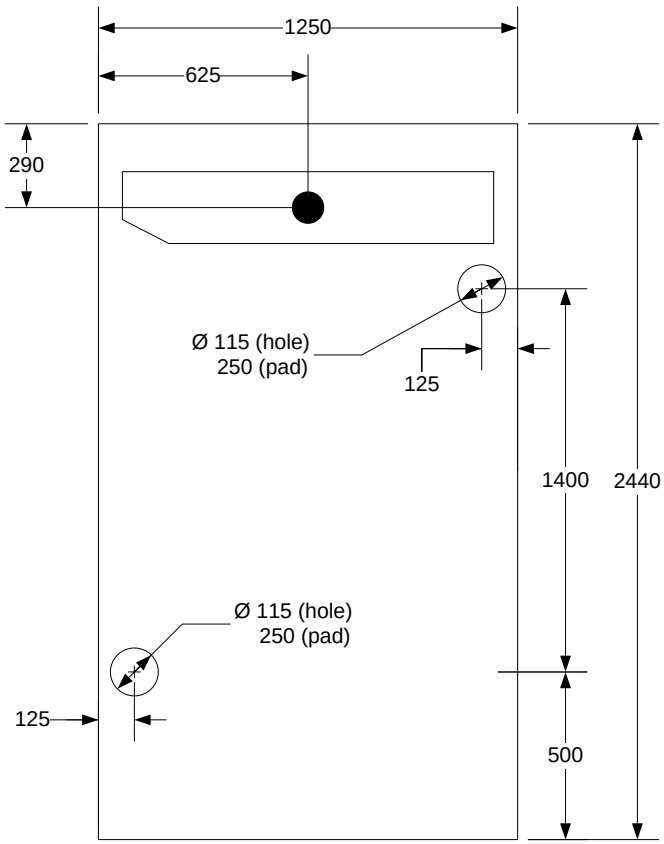
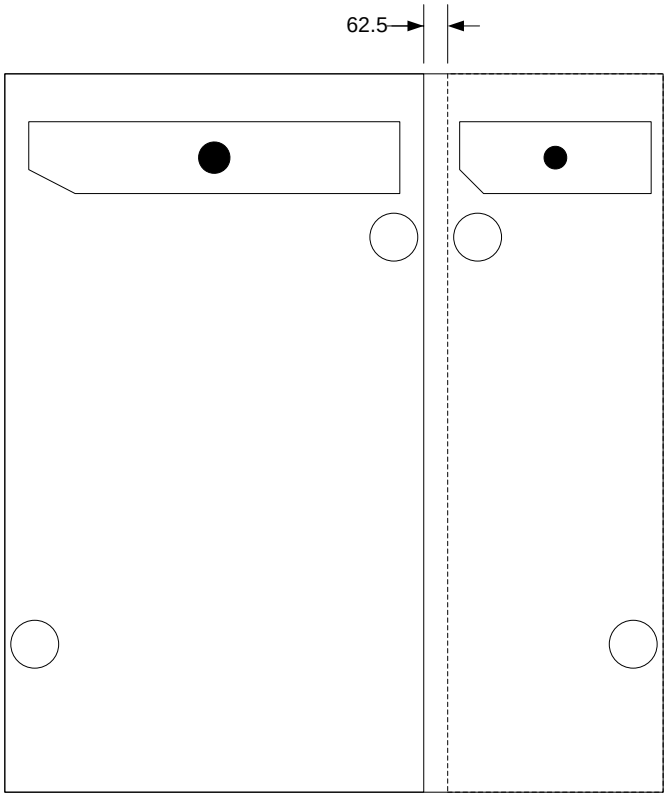
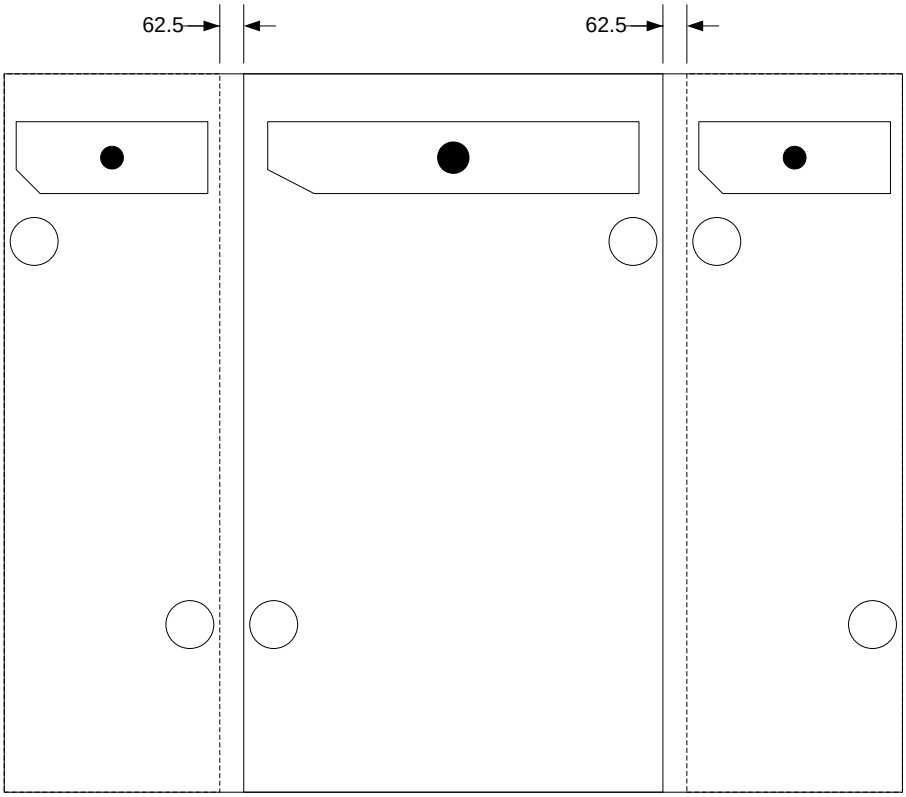


Figure 10: MDK-8 Mounting Hole, Size, and Hirose Connector location (units in mils)



BOTTOM VIEW

Figure 11: MDK-12 Alignment (MDK-4 and MDK-8 footprints separated by 62.5 mils)



BOTTOM VIEW

Figure 12: MDK-16 Alignment (MDK-4 and MDK-8 footprints separated by 62.5 mils)

In the vertical dimension, the base board to board spacing is 7 mm. The MDK-MB includes components underneath the area used by the MDK daughter boards. 4.5 mm has been reserved for use by these components. Therefore, MDK daughter boards must be designed requiring no more than 2.5 mm of clearance for bottom side mounted components. This is illustrated in Figure 13.

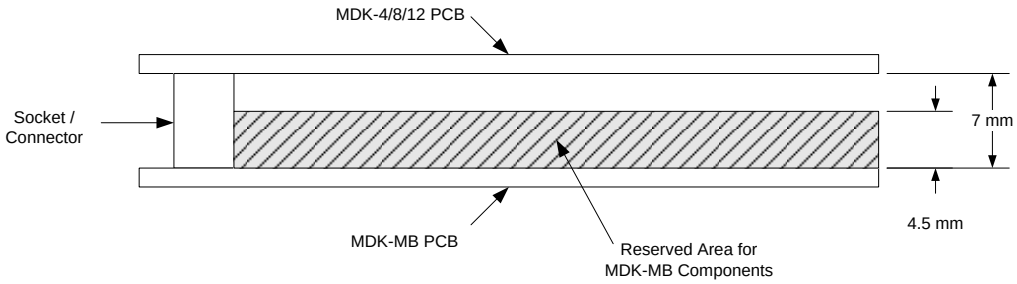


Figure 13: Required Bottom Clearance, MDK board designs

MityDSP Interface

Table 9: MityDSP/SO-DIMM Connector Assignments

Pin	I/O	Signal	Pin	I/O	Signal
A1	-	+3.3 V	B1	-	+3.3 V
A2	-	GND	B2	-	GND
A3	I	DSP_TMS	B3	I	MRESET#
A4	O	DSP_TDO	B4	I	DSP_TRST
A5	I	DSP_TDI	B5	I	DSP_EMU1
A6	I	DSP_TCK	B6	I	DSP_EMU0
A7	I	CLKS0	B7	I	CLKS1
A8	I/O	CLKR0	B8	I/O	CLKR1
A9	I/O	CLKX0	B9	I/O	CLKX1
A10	I	DR0	B10	I	DR1
A11	O	DX0	B11	O	DX1
A12	I/O	FSR0	B12	I/O	FSR1
A13	I/O	FSX0	B13	I/O	FSX1
A14	-	GND	B14	-	GND
A15	-	+1.23 V	B15	-	+1.23 V
A16	O	RESET#	B16	O	CLKOUT2
A17	O	RESET	B17	O	CLKOUT3
A18	-	GND	B18	-	GND
A19	I	FPGA_TCK	B19	O	FPGA_TDO
A20	I	FPGA_TDI	B20	I	FPGA_TMS
A21	I/O	DC1_IO9	B21	O	RS232_DBG_TXD
A22	I/O	DC1_IO10	B22	I	RS232_DBG_RXD
A23	I/O	DC1_IO11	B23	O	DI_LOAD
A24	I/O	DC1_IO0	B24	I/O	DC1_IO8
A25	I/O	DC1_IO1	B25	O	USB_TXD
A26	I/O	DC1_IO2	B26	I	USB_RXD
A27	I/O	DC1_IO3	B27	O	USB_RTS
A28	I/O	DC1_IO4	B28	I	USB_CTS
A29	I/O	DC1_IO5	B29	O	ADC_CS
A30	I/O	DC1_IO6	B30	O	RTC_SCL
A31	I/O	DC1_IO7	B31	I/O	RTC_SDA
A32	I/O	DC2_IO8	B32	I	DI_DAT
A33	I/O	DC2_IO9	B33	I/O	ETH_MDIO
A34	I/O	DC2_IO10	B34	O	ETH_MDC
A35	I/O	DC2_IO11	B35	O	25MHZ_REF_CLK
A36	I/O	DC4_IO0	B36	O	ETH_RESET#
A37	I/O	DC4_IO1	B37	I	ETH_RX_CLK
A38	I/O	DC4_IO2	B38	I	ETH_RX_DV
A39	I/O	DC4_IO3	B39	I	ETH_CRS
A40	I/O	DC4_IO4	B40	I	ETH_RX_ER
A41	I/O	DC4_IO5	B41	I	ETH_COL
A42	I/O	DC4_IO6	B42	I	ETH_RXD0
A43	I/O	DC4_IO7	B43	I	ETH_RXD1
A44	I/O	DC4_IO8	B44	I	ETH_RXD2
A45	I/O	DC4_IO9	B45	I	ETH_RXD3
A46	I/O	DC4_IO10	B46	I	ETH_TX_CLK
A47	I/O	DC4_IO11	B47	O	ETH_TX_EN
A48	I/O	DC3_IO0	B48	O	ETH_TXD0
A49	I/O	DC3_IO1	B49	O	ETH_TXD1

Pin	I/O	Signal	Pin	I/O	Signal
A50	I/O	DC3_IO2	B50	O	ETH_TXD2
A51	I/O	DC3_IO3	B51	O	ETH_TXD3
A52	I/O	DC3_IO4	B52	I/O	DC2_IO0
A53	I/O	DC3_IO5	B53	I/O	DC2_IO1
A54	I/O	DC3_IO6	B54	I/O	DC2_IO2
A55	I/O	DC3_IO7	B55	I/O	DC2_IO3
A56	I/O	DC3_IO8	B56	I/O	DC2_IO4
A57	I/O	DC3_IO9	B57	I/O	DC2_IO5
A58	I/O	DC3_IO10	B58	I/O	DC2_IO6
A59	I/O	DC3_IO11	B59	I/O	DC2_IO7
A60	-	GND	B60	-	GND
A61	O	DO_A3_P	B61	O	DISP_A0_P
A62	O	DO_A3_N	B62	O	DISP_A0_N
A63	O	DO_CLKIN_P	B63	O	DISP_A1_P
A64	O	DO_CLKIN_N	B64	O	DISP_A1_N
A65	O	DO_A2_P	B65	O	DISP_A2_P
A66	O	DO_A2_N	B66	O	DISP_A2_N
A67	O	DO_A1_P	B67	O	DISP_A3_P
A68	O	DO_A1_N	B68	O	DISP_A3_N
A69	O	DO_A0_P	B69	O	DISP_CLKIN_P
A70	O	DO_A0_N	B70	O	DISP_CLKIN_N
A71	-	GND	B71	-	GND
A72	-	+2.5 V	B72	-	+2.5 V

MDK Interface Cards

Table 10: MDK Off-The-Shelf Interface Cards (see www.mitydsp.com for latest list)

Card Number	Description / Features	MDK-4	MDK-8	MDK-12	MDK-16	MDK-24	Other
MDK4-RS232	Single RS-232 Interface Card with hardware flow control lines (no modem control) OR Dual RS-232 Interface without flow control	X					
MDK4-RS485	RS-485 Interface Card supporting 2 output and 2 input signaling lines.	X					
MDK4-SD	SD-FLASH interface card controller, SPIO mode.	X					
MDK4-TSA	Touch Screen Adaptor	X					
MDK8-ADS8239	1 Msps 16 bit Analog to Digital Converter utilizing ADS8239.		X				
MDK8-ADS8344	8 channel 16 bit 100 Msps Analog to Digital Converter utilizing ADS8344.		X				
MDK8-DIGIOISO	TTL Discrete Input/Output Interface Card, isolated inputs/outputs.		X				
MDK8-A3967	Independent dual axis stepper motor controller, micro-stepping down to 1/8 step size.		X				
MDK12-TTLIO	TTL Discrete Input/Output Interface Card			X			
MDK16-AWG	Analog Waveform Generator, dual summed 14 bit DACs, 100 Msps.				X		
MDK-QVGA-LCD	Quarter VGA LCD Display Adaptor, LVDS interface.						X

REVISION HISTORY

Date	Change Description
29-SEP-2009	Initial release of current spec.
28-MAR-2013	Revision history table added and header/footer updated.

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