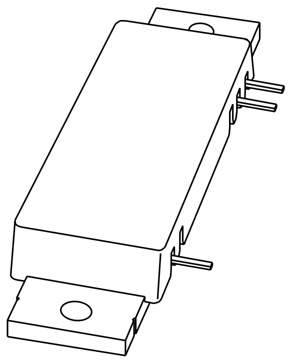
DATA SHEET



BGF944
GSM900 EDGE power module

Product specification
Supersedes data of 2003 Feb 26

2003 Jun 06

Philips
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GSM900 EDGE power module BGF944

FEATURES

- Typical GSM EDGE performance at a supply voltage of 26 V:
  - Output power = 2.5 W
  - Gain = 29 dB
  - Efficiency = 15%
  - ACPR < –65 dBc at 400 kHz
  - rms EVM < 0.4%
  - peak EVM < 1.2%
- Low distortion to a GSM EDGE signal
- Excellent 2-tone performance
- Low die temperature due to copper flange
- Integrated temperature compensated bias
- 50 Ω input/output impedance
- Flat gain over frequency band.

APPLICATIONS

- Base station RF power amplifiers in the 920 to 960 MHz frequency band
- GSM, GSM EDGE, multi carrier applications
- Macrocell (driver stage) and Microcell (final stage).

DESCRIPTION

17 W LDMOS power amplifier module for base station amplifier applications in the 920 to 960 MHz band.

PINNING - SOT365C

PIN	DESCRIPTION
1	RF input
2	V_S
3	RF output
Flange	ground

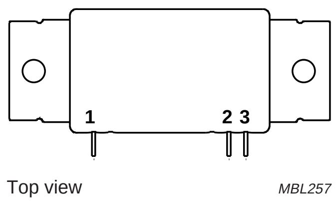


Fig.1 Simplified outline.

QUICK REFERENCE DATA

Typical RF performance at T_{mb} = 25 °C.

MODE OF OPERATION	f (MHz)	V_S (V)	P_L (W)	G_p (dB)	η (%)	ACPR (dBc)	rms EVM (%)
CW	920 to 960	26	17	28	47	–	–
GSM EDGE	920 to 960	26	2.5	29	15	–65[1]	0.4

Note

1. ACPR 400 kHz at 30 kHz resolution bandwidth.

MODE OF OPERATION	f (MHz)	V_S (V)	P_L (W)	G_p (dB)	d_3 (dB)	d_5 (dB)	d_7 (dB)
2-tone	920 to 960	26	2.5	29	–44	–52	–60

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_S	DC supply voltage	–	30	V
P_D	input drive power	–	100	mW
P_L	load power	–	24	W
T_{stg}	storage temperature	–30	+100	°C
T_{mb}	operating mounting base temperature	–20	+90	°C

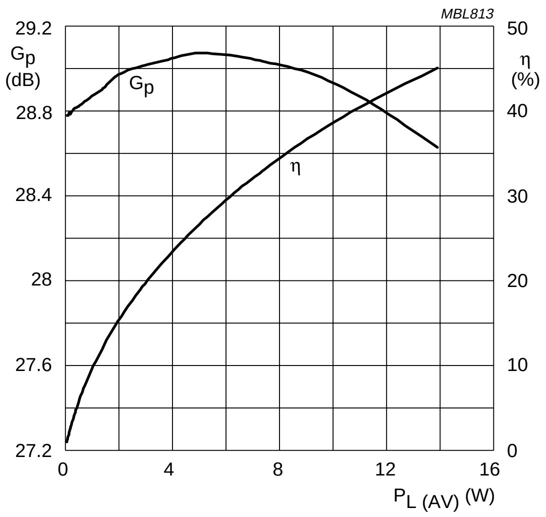
CHARACTERISTICS

T_{mb} = 25 °C; V_S = 26 V; P_L = 2.5 W; f = 920 to 960 MHz; $Z_S = Z_L$ = 50 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DQ}	quiescent current (pin 2)	P_D = 0 mW	–	280	320	mA
P_{1dB}	load power	at 1 dB gain compression	13	17	–	W
G_p	power gain		27	29	31	dB
$\Delta G_{p\ freq}$	gain flatness over frequency range		–	0.2	1	dB
$\Delta G_{p\ pwr}$	gain flatness over power band	P_L = 25 mW up to 2.5 W	–0.8	–0.2	+0.2	dB
G_{OB}	out of band gain	small signal, P_D = 0 dBm; f < 920 MHz, f > 960 MHz	–	–	$G_{Pi\ max}$ + 1 note 1	dB
$VSWR_{in}$	input VSWR		–	1.6 : 1	2 : 1	
IMD_r	reverse intermodulation	$f_i = f_c$ ±200 kHz; $P_{carrier}$ = 2.5 W; $P_{interference}$ = –40 dBc;	–	–66	–60	dBc
H_2	second harmonic		–	–38	–35	dBc
H_3	third harmonic		–	–61	–58	dBc
	stability	VSWR ≤ 3 : 1 through all phases; V_{S2} = 25 to 28 V	all spurious outputs more than 60 dB below desired signal			
	ruggedness	VSWR = 10 : 1 through all phases; P_L = 5 W	no degradation in output power			
EDGE (P_L = 2.5 W average)						
η	efficiency		12	15	–	%
SR200	spectral regrowth; EDGE GSM signal	200 kHz	–	–36	–35	dBc
SR400		400 kHz	–	–65	–63	dBc
EVM_{rms}	rms EDGE signal distortion		–	0.4	1.2	%
EVM_M	peak EDGE signal distortion		–	1.2	4	%
Intermodulation distortion (P_L = 2.5 W average)						
d_3	third order intermodulation	carrier spacing = 200 kHz	–	–45	–40	dBc
d_5	fifth order intermodulation		–	–52	–	dBc
d_7	seventh order intermodulation		–	–60	–	dBc

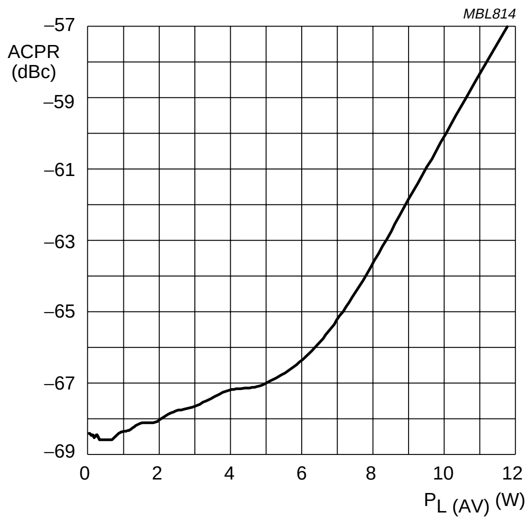
Note

1. G_{Pi} is small signal in-band gain.



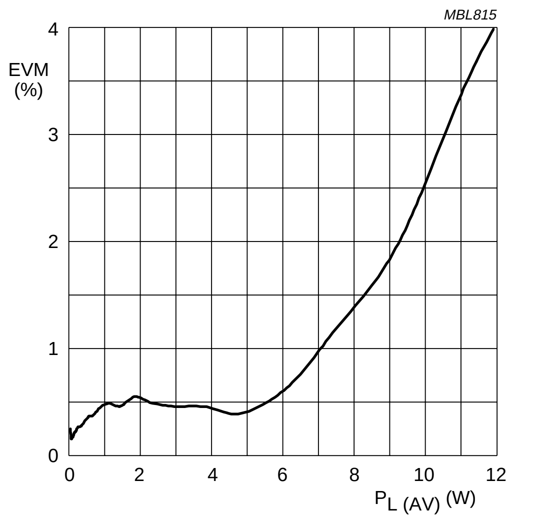
f = 940 MHz.

Fig.2 GSM EDGE power gain and efficiency as functions of load power; typical values.



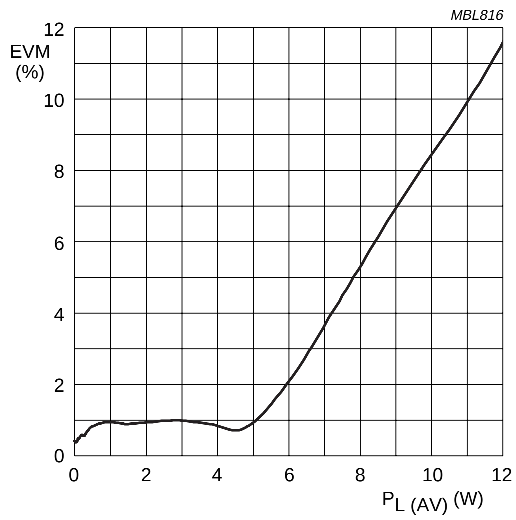
f = 940 MHz.

Fig.3 GSM EDGE ACPR at 400 kHz as a function of load power; typical values.



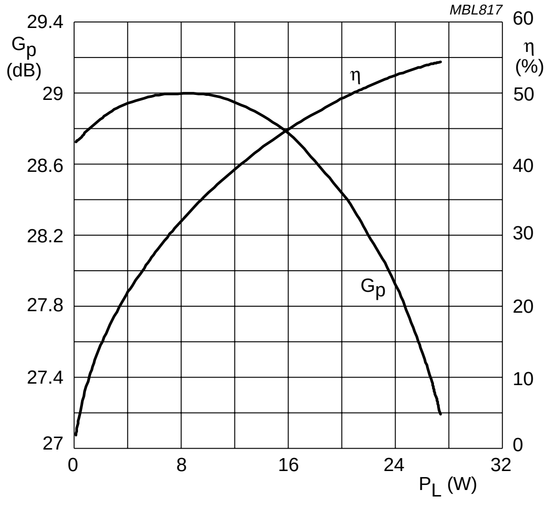
f = 940 MHz.

Fig.4 GSM EDGE rms EVM as a function of average load power; typical values.



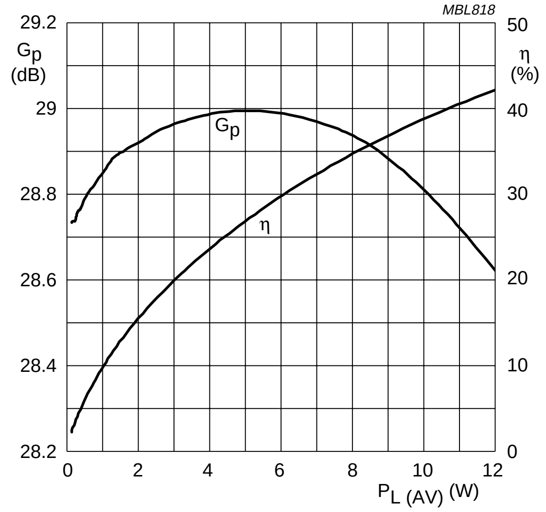
f = 940 MHz.

Fig.5 GSM EDGE peak EVM as function of average load power; typical values.



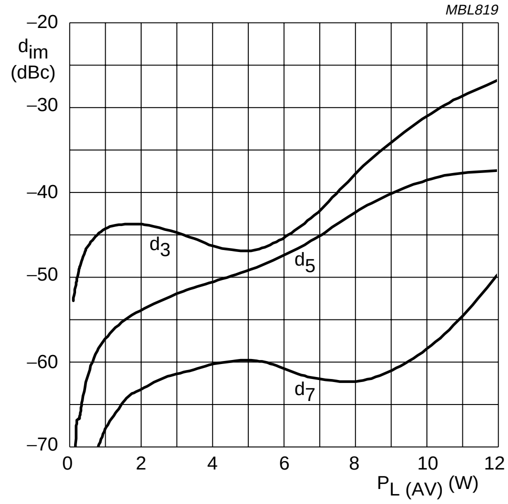
f = 940 MHz.

Fig.6 CW gain power and efficiency as functions of load power; typical values.



f_1 = 940 MHz; f_2 = 941 MHz.

Fig.7 Two tone gain power and efficiency as functions of load power; typical values.



f_1 = 940 MHz; f_2 = 941 MHz.

Fig.8 Two tone intermodulation distortion as a function of average load power; typical values.

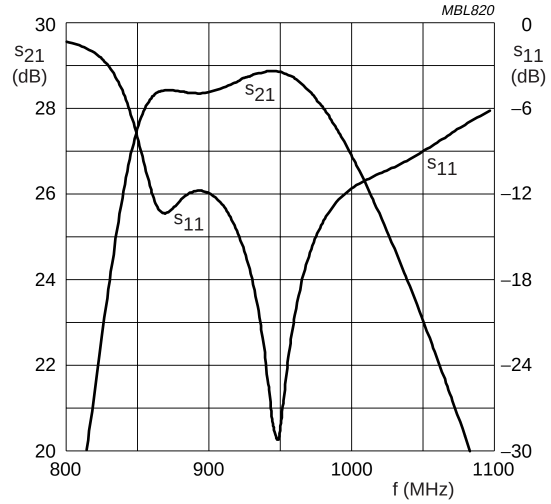


Fig.9 s-parameters as a function of frequency.

MOUNTING RECOMMENDATIONS

General

LDMOST base station modules are manufactured with the dies directly mounted onto a copper flange. The matching and bias circuit components are mounted on a printed-circuit board (PCB), which is also soldered onto the copper flange. The dies and the PCB are encapsulated in a plastic cap, and pins extending from the module provide a means of electrical connection. This construction allows the module to withstand a limited amount of flexing, although bending of the module is to be avoided as much as possible. Mechanical stress can occur if the bottom surface of the module and the surface of the amplifier casing (external heatsink) are not mutually flat. This, therefore, should be a consideration when mounting the module in the amplifier. Another cause of mechanical stress can arise from thermal mismatch after soldering of the pins. Precautions should be taken during soldering, and efforts made to ensure a good thermal contact between the flange and the external heatsink.

External heatsink (amplifier casing)

The module should always be mounted on a heatsink with a low thermal resistance to keep the module temperature as low as possible. The mounting area of the heatsink should be flat and free from burrs and loose particles. We recommend a flatness for the mounting area of between 50 µm concave and 50 µm convex. The 50 µm concave value is to ensure optimal thermal behaviour, while the 50 µm convex value is intended to limit mechanical stress due to bending.

In order to ensure optimal thermal behaviour, the use of thermal compound is recommended when mounting the module onto the amplifier external heatsink.

The following recommended thermal compounds have a thermal conductivity of >0.5 W/mK:

- WPS II (silicone-free) from Austerlitz-Electronics
- Comp. Trans. from KF
- 340 from Dow Corning
- Trans-Heat from E. Friis-Mikkelsen.

The use of thermal pads instead of thermal compound is not recommended as the pads may not maintain a uniform flatness over a period of time.

Mounting

PREPARATION

Ensure that the surface finishes are free from burrs, dirt and grease.

CAUTION

During the following procedures ESD precautions should be taken to protect the device from electrostatic damage.

PROCEDURE

1. Apply a thin, evenly spread layer of thermal compound to the module flange bottom surface. Excessive use of thermal compound may result in increased thermal resistance and possible bending of the of the flange. Too little thermal compound will result in an increase in thermal resistance.
2. Take care that there is some space between the cap and the PCB. Bring the module into contact with the external heatsink casing, ensuring that there is sufficient space for excessive thermal compound to escape.
3. Carefully align the module with the heatsink casing mounting holes, and secure with two 3 mm bolts and two flat washers. Initially tighten the bolts to “finger tight” (approximately 0.05 Nm). Using a torque wrench, tighten each bolt in alternating steps to a final torque of 0.4 Nm.
4. After the module is secured to the casing, the module leads may be soldered to the PCB. The leads are for electrical connection only, and should not be used to support the module at any time in the assembly process.

   A soldering iron may be used up to a temperature of 250 °C for a maximum of 10 seconds. Avoid contact between the soldering iron and the plastic cap.

Electrical connections

The main ground path of all modules is via the flange. It is therefore important that the flange is well grounded and that return paths are kept as short as possible.
An incorrectly grounded flange can result in a loss of output power or in oscillation.

The RF input and output of the module are designed for 50 Ω connections.

Incoming inspection

When incoming inspection is performed, use a properly designed test fixture to avoid excessive mechanical stress and to ensure optimal RF performance. Philips can deliver dedicated test fixtures on request.

APPLICATION INFORMATION

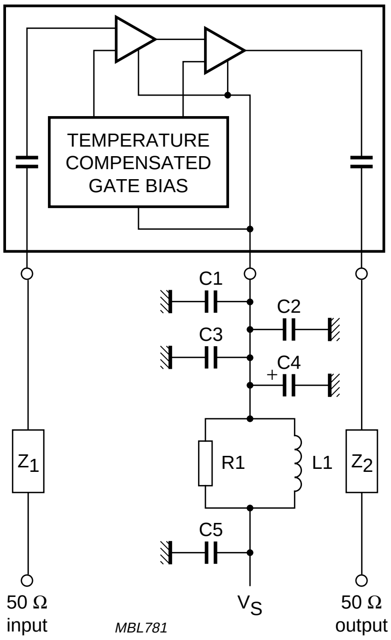


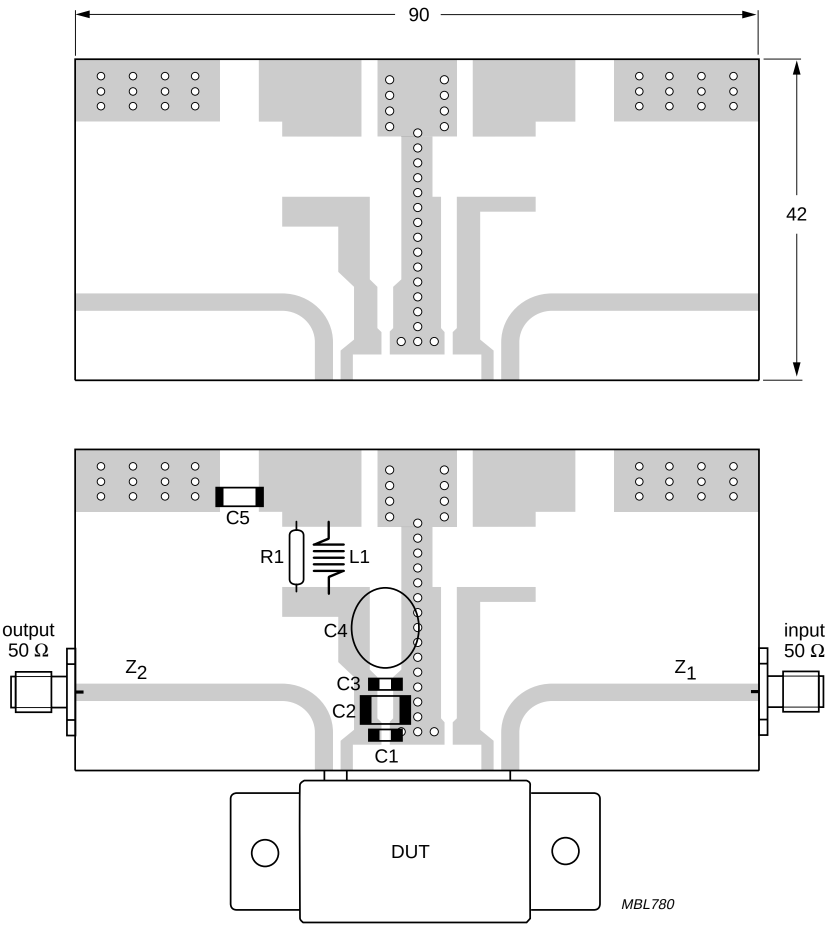
Fig.10 Test circuit.

List of components (see Figs 10 and 11)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NUMBER
C1, C3	multilayer X7R ceramic chip capacitor	100 nF; 50 V	
C2, C5	tantalum SMD capacitor	10 μF; 35 V	
C4	electrolytic capacitor	100 μF; 35 V	
L1	grade 4S2 Ferroxcube bead		4330 030 36300
R1	metal film resistor	10 Ω; 0.4 W	2322 195 13109
Z_1, Z_2	stripline; note 1	50 Ω	

Note

1. The striplines are on a double copper-clad printed-circuit board (RO5880) with ε_r = 2.2 and thickness = 0.79 mm.

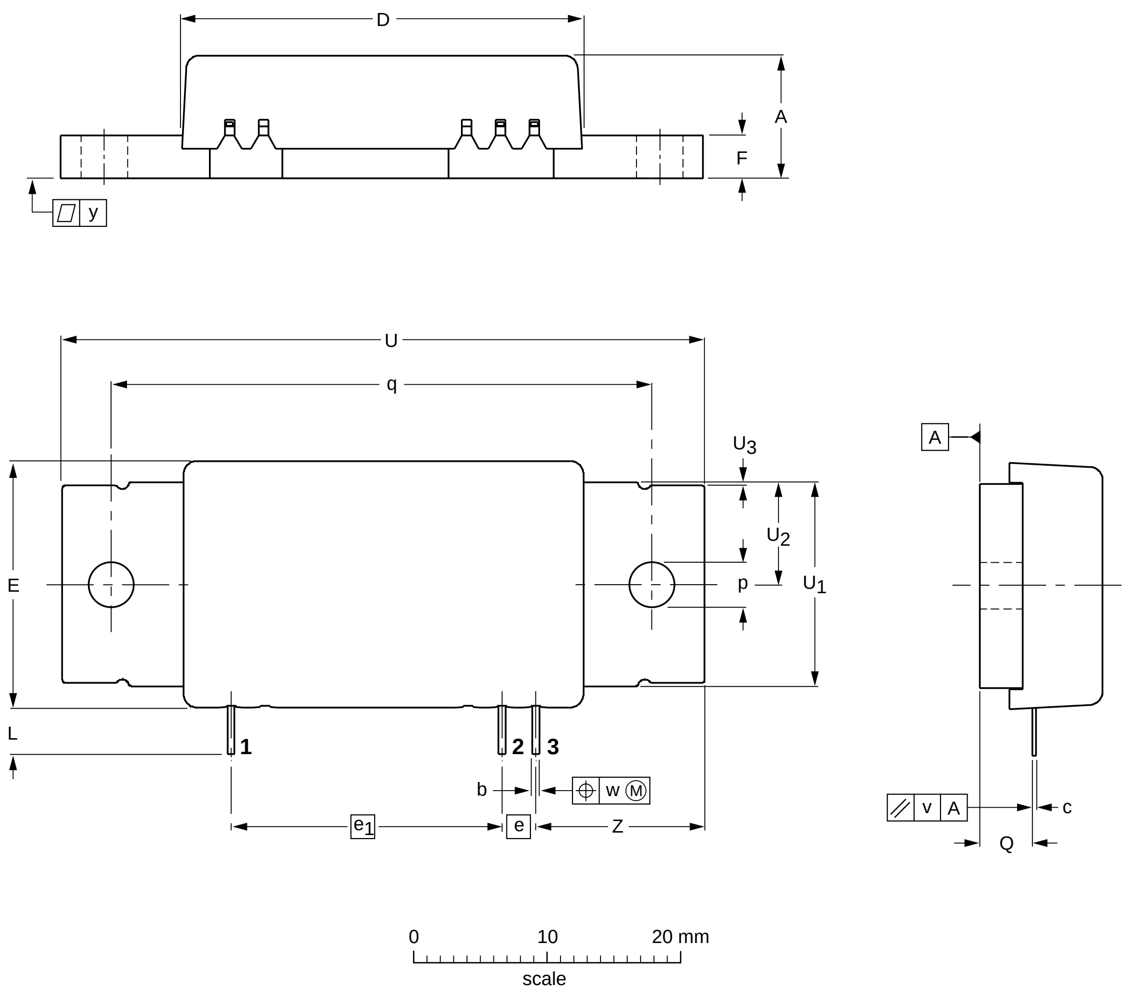


Dimensions in mm.

Fig.11 Printed-circuit board and component layout.

PACKAGE OUTLINE

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 3 in-line leads SOT365C



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	e_1	F	L	p	Q	q	U	U_1	U_2	U_3	v	w	y	Z
mm	9.5 9.0	0.56 0.46	0.3 0.2	30.1 29.9	18.6 18.4	2.54	20.32	3.3 3.1	3.7 3.3	3.55 3.45	4.0 3.8	41.75 41.65	48.4 48.0	15.4 15.2	7.75 7.55	1.1 0.0	0.3	0.25	0.1	12.8 12.6

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT365C						~~01-06-06~~ 02-11-13

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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