GENERAL DESCRIPTION

Tethys™ 4192 is optimized for SONET/SDH applications as a full-duplex two STS-192/STM-64 MUX/DEMUX with full framer functionality including pointer processing, and overhead termination; ideal for aggregation, ADM and DWDM applications. In the demultiplex ingress direction, Tethys™ 4192 accepts two STS-192/STM-64 signals in SFI-4.1 format. Tethys locates the incoming SONET/SDH frame, optionally descrambles the data, monitors theTOH and POH, and provides STS-1 level pointer processing. In addition, Tethys supports TOH and POH overhead transparency.

In the multiplex direction, from the system interface, Tethys™ 4192 accepts two STS-192/STM-64 or eight STS-48/STM-16 signals in either dual 4 x 2.5 Gbit/s or 8 serial 2.5 Gbit/s format. Further Tethys provides corresponding functionality in the DEMUX direction.

APPLICATIONS

- ADM
- Metro Aggregation
- Digital Cross Connects
- Repeaters
- DWDM Equipment
- Test Equipment

FEATURES

- Complies with OIF specifications SFI-4.1
- Differential CML 2.5 G I/O interface to system/backplane
- TFI-5 Support
- Processes SONET/SDH dual STS-192/STM-64 on the line side interface
- Processes SONET/SDH dual STS-192/STM-64 or eight STS-48/STM-16 on the system/client side serial 2.5 Gbit/s interface
- Provides line timing of all line and system side interfaces
- Processes SONET/SDH flexible concatenation streams of STS-2c, 3c, 4c, … to 192c
- Supports auto-detection of concatenation streams STS-3c/STM-1, STS-12c/STM-4, STS-48c/STM-16 and STS-192c/STM-64
- Supports STS-1 level pointer processing of STS-192/STM-64 or STS-48/STM-16 streams
- Provides interfaces for dropping alarm and status information, and for forcing alarm conditions
- Supports system-side input deskew of up to ± 250 ns within a group of 4 x 2.5G GBps for each of two STS-192/STM-64
- Power dissipation of 15 W, depending on mode of operation
- Terminates and generates SONET section, line, and path layers
- Provides TOH and POH transparency
- Provides monitoring of POH bytes B3 and N1/Z5
- Provides B2 SF/SD capability for Poisson and bursty error distribution
- Provides full TOH/POH add/drop
- Provides STS-1 level POH add/drop
- Supports more than ± 746 UI programmable output skew on STS-192/STM-64 or STS-48/STM-16 out-put links to external cross-connects
- For diagnostic purposes, Tethys provides PRBS generator/checker and loop backs
- Provides B1, B2, H1 and H2 bit error generation for both receive and transmit direction diagnostics
- Provides 1 second performance monitors
- Provides B1, B2, H1 and H2 bit error generation for both receive and transmit direction diagnostics
- Provides 1 second performance monitors
- 0.13 micron process, 1.2 V core, 3.3 V I/O
- Motorola 32-bit synchronous microprocessor inter-face for configuration, control, and status monitoring
- Complies with GR-253, GR-1377, ITU-T G.707, and ANSI T1.105
- Provides a standard 5-signal IEEE 1149.1 JTAG test port for boundary scan board test purposes

SPECIFICATIONS

- OIF SFI-4.1
- OIF TFI-5

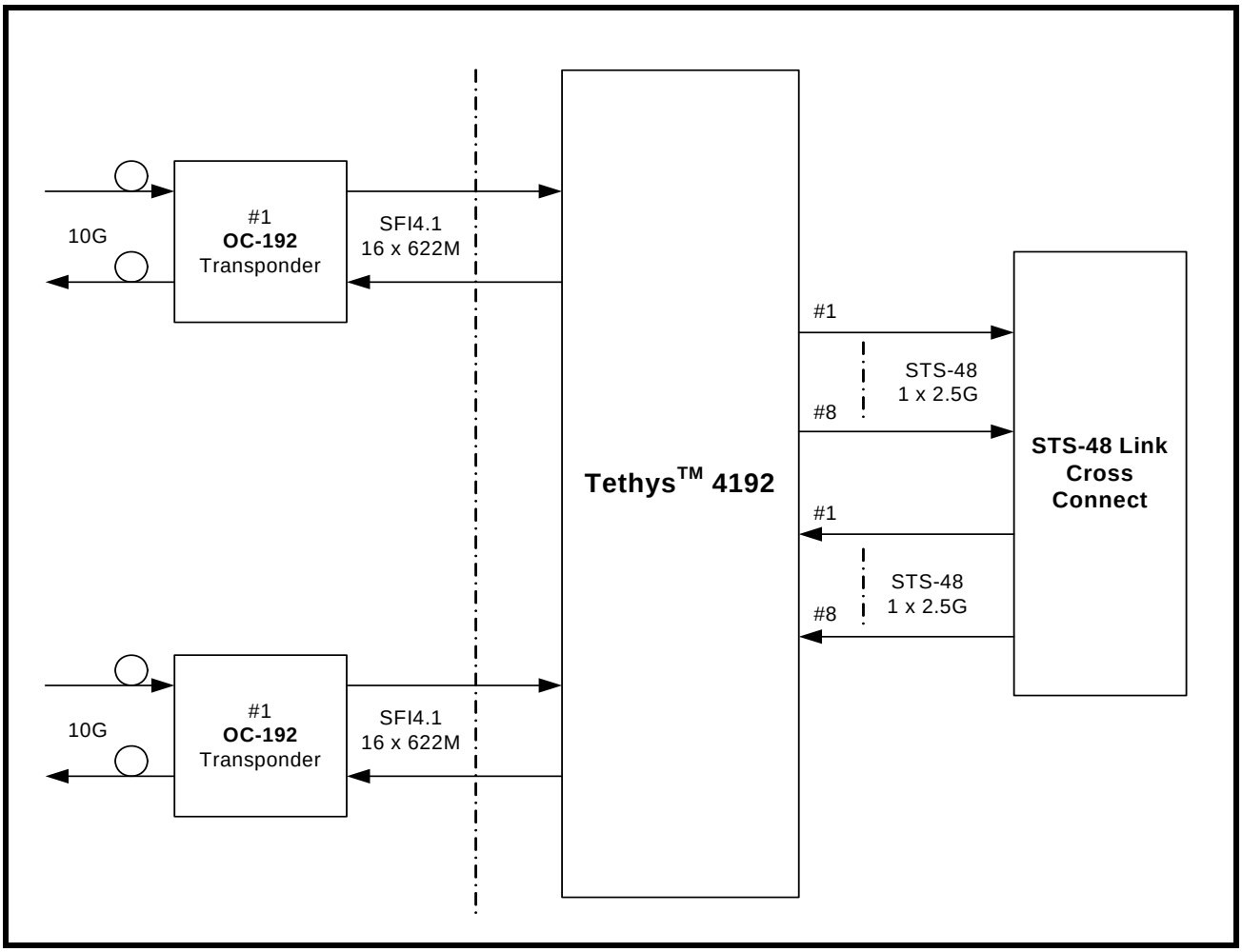
STANDARDS

- ANSI T1.105-2000-193R2 (DRAFT)
- ANSI T1.105.05-1994
- T1X1.3/93-005RI -1993 - preliminary
- GR-253-CORE Sept. 2000
- ITU-T G.707 10/2000

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
PEB1756E	1397 CBGA	-40°C to +85°C

FIGURE 1. PEB1757E APPLICATION DIAGRAM



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