

# CY62256VN

# 256-Kbit (32 K × 8) Static RAM

#### Features

- Temperature ranges □ Commercial: 0 °C to +70 °C □ Industrial: -40 °C to +85 °C □ Automotive-A: -40 °C to +85 °C □ Automotive-E: -40 °C to +125 °C
- Speed: 70 ns
- Low voltage range: 2.7 V to 3.6 V
- Low active power and standby power
- Easy memory expansion with CE and OE features
- TTL compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Available in standard Pb-free and non Pb-free 28-pin (300-mil) narrow SOIC, 28-pin TSOP-I, and 28-pin reverse TSOP-I packages

#### **Functional Description**

The CY62256VN family is composed of two high performance CMOS static RAM's organized as 32K words by 8 bits. Easy <u>memory</u> expansion is provided by an <u>active LOW</u> chip enable  $(\overline{CE})$  and active LOW output enable  $(\overline{OE})$  and tristate drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected.

An active LOW write enable signal ( $\overline{\text{WE}}$ ) controls the writing/reading operation of the memory. When  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  active LOW, while  $\overline{\text{WE}}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH.

For a complete list of related documentation, click here.



#### Logic Block Diagram

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# CY62256VN

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#### **Product Portfolio**

		V <sub>CC</sub> Range (V)			Power Dissipation				
Product	Range				Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (µA)		
		Min Typ <sup>[1]</sup> Max		<b>Typ</b> <sup>[1]</sup>	Max	<b>Typ</b> <sup>[1]</sup>	Max		
CY62256VNLL	Commercial	2.7	3.0	3.6	11	30	0.1	5	
CY62256VNLL	Industrial	2.7	3.0	3.6	11	30	0.1	10	
CY62256VNLL	Automotive-A	2.7	3.0	3.6	11	30	0.1	10	
CY62256VNLL	Automotive-E	2.7	3.0	3.6	11	30	0.1	130	

#### **Pin Configurations**

Figure 1. 28-pin SOIC and 28-pin TSOP I pinouts

#### **Narrow SOIC Top View** 8 1 A12 9 1 A13 10 1 1 1/O<sub>2</sub> 12 1 1/O<sub>2</sub> 13 1 1/O<sub>2</sub> 14 1 GND 15 1 1/O<sub>3</sub> 14 1 GND 15 1 1/O<sub>3</sub> 17 1 1/O<sub>4</sub> 19 1 1/O<sub>5</sub> 19 1 1/O<sub>5</sub> 19 1 1/O<sub>5</sub> 28 <u>VCC</u> A5 🗌 <sup>1</sup>0 <sup>22</sup> 23 7 21 OE 1 22 A1 224 A3 44 WE D 1 26 VCC 4 A3 44 WE D 1 28 VCC 4 A6 0 1 4 A7 0 1 4 A6 0 1 4 A7 0 14 A7 0 1 $A_0$ A<sub>6</sub> [ A<sub>7</sub> [ 27 🗌 WE 2 20 6 3 26 🛛 A4 5 A8 🗆 4 3 4 25 🛛 A3 $1/O_{6}$ $17 | I/O_{5}$ $16 | I/O_{4}$ $15 | I/O_{3}$ 14 | GND $13 | I/O_{2}$ 24 A2 23 A1 Ag 🛛 5 TSOP I TSOP I 2 A1006 **Reverse Pinout Top View** ) 1 28 27 26 25 24 23 22 🗌 OE A11 7 **Top View** (not to scale) 21 🛛 A<sub>0</sub> A12 8 (not to scale) A13 [ 9 A14 [ 10 I/O<sub>0</sub> [ 11 I/O<sub>1</sub> [ 12 I/O<sub>2</sub> [ 13 20 ] CE 19 | 1/07 18 | 1/06 A<sub>14</sub> A<sub>13</sub> A<sub>12</sub> 22 0 21 A 17 1/05 16 I/O4 15 I/O3 GND C 14

#### **Pin Definitions**

Pin Number	Туре	Description
1–10, 21, 23–26	Input	A <sub>0</sub> -A <sub>14</sub> . Address inputs
11–13, 15–19	Input/Output	I/O <sub>0</sub> -I/O <sub>7</sub> . Data lines. Used as input or output lines depending on operation.
27	Input/Control	WE. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
20	Input/Control	CE. When LOW, selects the chip. When HIGH, deselects the chip.
22	Input/Control	<b>OE</b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins.
14	Ground	GND. Ground for the device
28	Power Supply	V <sub>CC</sub> . Power supply for the device

#### Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}$  Typ,  $T_A = 25$  °C, and  $t_{AA} = 70$  ns.



#### **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature65 °C to +150 °C
Ambient temperature with power applied
Supply voltage to ground potential (pin 28 to pin 14) $^{[2]}$ 0.5 V to +4.6 V
DC voltage applied to outputs in high Z State $^{[2]}$ 0.5 V to V_{CC} + 0.5 V
DC input voltage $^{[2]}$ 0.5 V to V_{CC} + 0.5 V
Output current into outputs (LOW)20 mA

Static discharge voltage	
(per MIL-STD-883, method 3015)	> 2001 V
Latch-up current	

#### **Operating Range**

Device	Range	Ambient Temperature (T <sub>A</sub> ) <sup>[3]</sup>	V <sub>CC</sub>
CY62256VN	Commercial	0 °C to +70 °C	2.7 V to
	Industrial	–40 °C to +85 °C	3.6 V
	Automotive-A	–40 °C to +85 °C	
	Automotive-E	–40 °C to +125 °C	

# **Electrical Characteristics**

Over the Operating Range

Devenueter	Description	Test Cand	ltione		-70		L Init
Parameter	Description	Test Cond	Test Conditions		Тур <sup>[4]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -1.0 mA	$V_{CC} = 2.7 V$	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 2.1 mA	$V_{CC} = 2.7 V$	_	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.2	-	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage			-0.5	-	0.8	V
I <sub>IX</sub> Input leaka	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	Commercial/ Industrial/ Automotive-A	-1	_	+1	μΑ
			Automotive-E	-10	-	+10	μΑ
I <sub>OZ</sub>	Output leakage current	$\begin{array}{l} GND \leq V_{IN} \leq V_{CC}, \\ Output \ Disabled \end{array}$	Commercial/ Industrial/ Automotive-A	-1	_	+1	μA
			Automotive-E	-10	_	+10	μA
Icc	V <sub>CC</sub> operating supply current	$V_{CC} = 3.6 \text{ V},$ $I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$	All ranges	-	11	30	mA
I <sub>SB1</sub>	Automatic CE power-down current - TTL inputs	$\label{eq:constraint} \begin{array}{l} \frac{V_{CC}}{CE} = 3.6 \text{ V},\\ \overline{CE} \geq V_{IH},\\ V_{IN} \geq V_{IH} \text{ or }\\ V_{IN} \leq V_{IL},\\ f = f_{MAX} \end{array}$	All ranges	_	100	300	μΑ
I <sub>SB2</sub>	Automatic CE power-down	$V_{\rm CC} = 3.6  \text{V},$	Commercial	-	0.1	5	μΑ
	current - CMOS inputs	$\label{eq:cell} \begin{array}{l} \overline{CE} \geq V_{CC} - 0.3 \text{ V}, \\ V_{IN} \geq V_{CC} - 0.3 \text{ V or} \\ V_{IN} \leq 0.3 \text{ V}, \text{ f} = 0 \end{array}$	Industrial/ Automotive-A	-		10	
			Automotive-E	_		130	

V<sub>IL</sub>(min) = -2.0 V for pulse durations of less than 20 ns.
 T<sub>A</sub> is the "Instant-On" case temperature.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25 °C, and t<sub>AA</sub> = 70 ns.



# Capacitance

Parameter <sup>[5]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.0 \text{ V}$	6	pF
C <sub>OUT</sub>	Output capacitance		8	pF

#### **Thermal Resistance**

Parameter <sup>[5]</sup>	Description	Test Conditions	SOIC	TSOPI	RTSOPI	Unit
$\theta_{JA}$	(junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer	68.45	87.62	87.62	°C/W
θ <sup>JC</sup>	Thermal resistance (junction to case)	printed circuit board	26.94	23.73	23.73	°C/W

# **AC Test Loads and Waveforms**



Parameter	Value	Units
R1	1100	Ohms
R2	1500	Ohms
RTH	645	Ohms
VTH	1.750	Volts

5. Tested initially and after any design or process changes that may affect these parameters.



# **Data Retention Characteristics**

#### Over the Operating Range

Parameter	Description	Conditions <sup>[6]</sup>		Min	Тур [7]	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention			1.4	-	-	V
I <sub>CCDR</sub>	Data retention current	$\frac{V_{CC}}{V_{CC}} = 1.4 \text{ V},$	Commercial	-	0.1	3	μΑ
		$\begin{array}{l} \frac{V_{CC}}{CE} = 1.4 \text{ V},\\ CE \geq V_{CC} - 0.3 \text{ V},\\ V_{IN} \geq V_{CC} - 0.3 \text{ V}\\ \text{or } V_{IN} \leq 0.3 \text{ V} \end{array}$	Industrial/ Automotive-A	_		6	
		01 VIN <u>~</u> 0.0 V	Automotive-E	-		50	
t <sub>CDR</sub> <sup>[6]</sup>	Chip deselect to data retention time			0	-	-	ns
t <sub>R</sub> <sup>[8]</sup>	Operation recovery time			70	_	_	ns

#### **Data Retention Waveform**

#### Figure 3. Data Retention Waveform



- 6. No input may exceed  $V_{CC}$  + 0.3 V. 7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC}$  =  $V_{CC}$  Typ,  $T_A$  = 25 °C, and  $t_{AA}$  = 70 ns. 8. Tested initially and after any design or process changes that may affect these parameters.



# **Switching Characteristics**

Over the Operating Range

Parameter <sup>[9]</sup>	Description	CY622	CY62256VN-70	
Parameter	Description		Max	Unit
Read Cycle		·		
t <sub>RC</sub>	Read cycle time	70	-	ns
t <sub>AA</sub>	Address to data valid	-	70	ns
t <sub>OHA</sub>	Data hold from address change	10	-	ns
t <sub>ACE</sub>	CE LOW to data valid	-	70	ns
t <sub>DOE</sub>	OE LOW to data valid	-	35	ns
t <sub>LZOE</sub>	OE LOW to low Z <sup>[10]</sup>	5	-	ns
t <sub>HZOE</sub>	OE HIGH to high Z <sup>[10, 11]</sup>	-	25	ns
t <sub>LZCE</sub>	CE LOW to low Z <sup>[10]</sup>	10	-	ns
t <sub>HZCE</sub>	CE HIGH to high Z <sup>[10, 11]</sup>	-	25	ns
t <sub>PU</sub>	CE LOW to power-up	0	-	ns
t <sub>PD</sub>	CE HIGH to power-down	-	70	ns
Write Cycle [12	, 13]			
t <sub>WC</sub>	Write cycle time	70	-	ns
t <sub>SCE</sub>	CE LOW to write end	60	-	ns
t <sub>AW</sub>	Address setup to write end	60	-	ns
t <sub>HA</sub>	Address hold from write end		-	ns
t <sub>SA</sub>	Address setup to write start	0	-	ns
t <sub>PWE</sub>	WE pulse width	50	-	ns
t <sub>SD</sub>	Data setup to write end	30	-	ns
t <sub>HD</sub>	Data hold from write end	0	-	ns
t <sub>HZWE</sub>	WE LOW to high Z <sup>[10, 11]</sup>	-	25	ns
t <sub>LZWE</sub>	WE HIGH to low Z <sup>[10]</sup>	10	-	ns

Notes

Test conditions assume signal transition time of 5 ns or less timing reference levels of V<sub>CC</sub>/2, input pulse levels of 0 to V<sub>CC</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100-pF load capacitance.

10. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
11. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in (b) of <u>AC</u> Test Loads. Transition is measured ± 200 mV from steady-state voltage.
12. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should <u>be</u> referenced to the rising edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 3 (WE Controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.



Switching Waveforms



- Notes

  14. Device is continuously selected. OE, CE = V<sub>IL</sub>.
  15. WE is HIGH for read cycle.
  16. Address valid prior to or coincident with CE transition LOW.
  17. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
  18. Data I/O is high impedance if OE = V<sub>IL</sub>.
  19. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.
  20. During this period, the I/Os are in output state and input signals should not be applied.

- 20. During this period, the I/Os are in output state and input signals should not be applied.



#### Switching Waveforms (continued)



Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) <sup>[23, 24]</sup>



- 21. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

- 22. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ . 23. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state. 24. The minimum write cycle time for write cycle No. 3 (WE Controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>. 25. During this period, the I/Os are in output state and input signals should not be applied.





### **Typical DC and AC Characteristics**





# Typical DC and AC Characteristics (continued)





#### Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
Н	Х	Х	High Z	Deselect/power-down	Standby (I <sub>SB</sub> )
L	Н	L	Data out	Read	Active (I <sub>CC</sub> )
L	L	Х	Data in	Write	Active (I <sub>CC</sub> )
L	Н	Н	High Z	Deselect, output disabled	Active (I <sub>CC</sub> )



### **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62256VNLL-70ZXC	51-85071	28-pin TSOP I (Pb-free)	Commercial
	CY62256VNLL-70SNXI	51-85092	28-pin SNC (300 Mils) Narrow Body (Pb-free)	Industrial
	CY62256VNLL-70ZXI	51-85071	28-pin TSOP I (Pb-free)	
	CY62256VNLL-70ZRXI	51-85074	28-pin Reverse TSOP I (Pb-free)	
	CY62256VNLL-70SNXE	51-85092	28-pin SNC (300 Mils) Narrow Body (Pb-free)	Automotive-E
	CY62256VNLL-70ZXE	51-85071	28-pin TSOP I (Pb-free)	]

#### **Ordering Code Definitions**





#### **Package Diagrams**

Figure 9. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092



51-85092 \*E





51-85071 \*J

MAX. MIN.



#### **Package Diagrams**





51-85074 \*H



# Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

#### **Document Conventions**

#### Units of Measure

Symbol	Unit of Measure		
°C	degree Celsius		
μΑ	microampere		
mA	milliampere		
MHz	megahertz		
ns	nanosecond		
Ω	ohm		
pF	picofarad		
V	volt		
W	watt		





# **Document History Page**

Document Title: CY62256VN, 256-Kbit (32 K × 8) Static RAM Document Number: 001-06512				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	426504	NXR	See ECN	New data sheet
*A	488954	NXR	See ECN	Added Automotive product Updated ordering Information table
*В	2769239	VKN/AESA	09/25/09	Corrected V <sub>IL</sub> description in the Electrical Characteristics table
*C	2901521	AJU	03/30/2010	Removed inactive parts from Ordering Information. Updated Package Diagram.
*D	3119519	AJU	01/04/2011	Updated Ordering Information. Added Ordering Code Definitions.
*E	3329873	RAME	07/27/11	Updated template and styles according to current Cypress standards. Added acronyms and units. Removed reference to AN1064 SRAM system guidelines. Updated operation recovery time parameter under Data Retention Characteristics on page 6.
*F	4122787	VINI	09/13/2013	Updated Package Diagrams: spec 51-85092 – Changed revision from *C to *E. Updated in new template. Completing Sunset Review.
*G	4525875	VINI	10/06/2014	Updated Maximum Ratings: Referred Note 2 in "Supply voltage to ground potential (pin 28 to pin 14)". Updated Package Diagrams: spec 51-85071 – Changed revision from *I to *J. spec 51-85074 – Changed revision from *G to *H. Completing Sunset Review.
*H	4576406	VINI	01/16/2015	Added related documentation hyperlink in page 1. Added Note 13 in Switching Characteristics. Added note reference 13 in the Switching Characteristics table.



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