

Spread Spectrum Clock Generator

Features

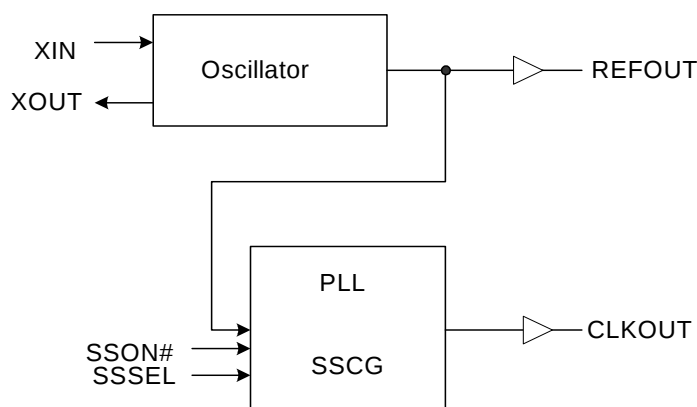
- Supports clock requirements for printers
- 48-MHz spread spectrum clock output
- 48-MHz reference clock output
- Two selectable spread percentages: –1% and –3%
- Integrated loop filter
- 48-MHz crystal or external clock input
- 3.3-V supply operation (2.5-V functional)
- 8-pin small outline integrated circuit (SOIC) package

Functional Description

The CY27020 clock generator provides a low EMI clock output for printers. It features spread spectrum technology, a modulation technique designed specifically for reducing EMI at the fundamental frequency and its harmonics.

For a complete list of related documentation, click [here](#).

Logic Block Diagram

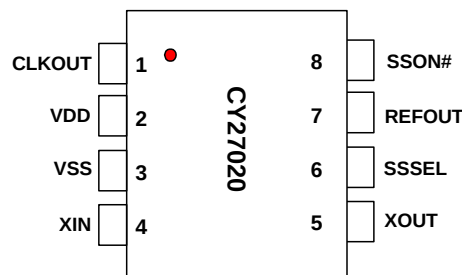


Frequency Table

XIN	SSON#	SSEL	REFOUT	CLKOUT
48.00 MHz	0	0	48.00 MHz	48.00 MHz at –1%
48.00 MHz	0	1	48.00 MHz	48.00 MHz at –3%
48.00 MHz	1	0	48.00 MHz	48.00 MHz (No Spread)
48.00 MHz	1	1	48.00 MHz	48.00 MHz (No Spread)

Pin Configuration

Figure 1. 8-pin SOIC pinout



Pin Description

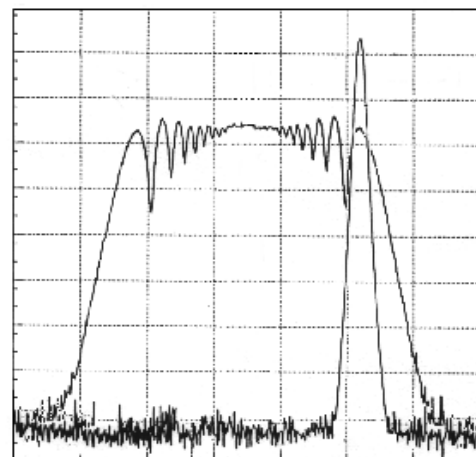
Pin	Name	I/o	Type ^[1]	Description
1	CLKOUT	O		Fixed frequency 48.00 MHz spread spectrum clock output. See Table on page 1 for frequency selections
2	VDD	PWR		3.3-V power supply
3	VSS	PWR		Ground
4	XIN	I		Oscillator buffer input. Connect to an external parallel resonant crystal (nominally 48.00 MHz) or externally generated 48 MHz reference clock.
5	XOUT	O		Oscillator buffer output. Connect to an external parallel resonant crystal. Do not connect when an externally generated reference clock is applied at XIN.
6	SSSEL	I	PU	Spread spectrum percentage select input. See Table on page 1 for details.
7	REFOUT	O	–	Buffered output of XIN.
8	SSON#	I	PD	Spread spectrum enable input. When asserted LOW, spread spectrum is enabled.

Spread Spectrum Clock Generation (SSCG)

Spread spectrum clock generation (SSCG) is a frequency modulation technique used to reduce electromagnetic interference radiation generated by repetitive digital signals, mainly clocks. A clock accumulates electromagnetic energy at its center frequency and its harmonics. Spread spectrum distributes this energy over a small frequency band and decreases the peak value of radiated energy over the spectrum. This technique is achieved by modulating the clock around or below the center of its nominal frequency by a certain percentage (which also determines the energy distribution band).

The SSCG function is enabled when SSON# pin is asserted low, resulting in a spread bandwidth that is down spread by either –1% or –3%, selected by SSSEL (see [Table on page 1](#)).

Figure 2. No Spread vs Down Spread Example



Note

1. PU = Internal pull-up resistor, PD = Internal pull-down resistor.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.^[2]

Minimum input voltage relative to V_{SS} : $V_{SS} - 0.3 \text{ V}$

Maximum input voltage relative to V_{DD} : $V_{DD} + 0.3 \text{ V}$

Storage temperature: -65°C to 150°C

Operating temperature: 0°C to 70°C

Maximum electrostatic discharge (ESD) protection: 2 kV

Maximum power supply: 5.5 V

Operating voltage: 2.5 V–3.6 V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, care should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, the I/O pins should be constrained to the range:

$$V_{SS} < I/O < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications

($V_{DD} = 3.3 \text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to 70°C)^[3]

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage	SSON#, SSSEL	–	–	0.8	V
V_{IH}	Input high voltage		2.2	–	–	V
V_{thXIN}	XIN threshold voltage		$0.3 \times V_{DD}$	$0.5 \times V_{DD}$	$0.7 \times V_{DD}$	V
I_{IL1}	Input low current	SSON# = V_{SS}	–5	0	5	μA
I_{IH1}	Input high current	SSON# = V_{DD}	3	8	20	μA
I_{IL2}	Input low current	SSEL = V_{SS}	–36	–16.5	–7.4	μA
I_{IH2}	Input high current	SSEL = V_{DD}	–5	0	5	μA
$I_{DD3.3V}$	Dynamic supply current	No output load	–	20	25	mA
V_{OL}	Output low voltage	$I_{OL} = 4.0 \text{ mA}$	–	–	0.4	V
V_{OH}	Output high voltage	$I_{OH} = -4.0 \text{ mA}$	2.4	–	–	V
C_{in}	Input capacitance	Pins 6 and 8	–	3	5	pF
C_x	XIN, XOUT capacitance	Pins 4 and 5	–	3	5	pF
PU/PD	Pull-up/pull-down resistance	SSON#, SSSEL	100	200	400	$\text{k}\Omega$

Notes

- Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- In applications where a crystal is used for the input reference clock, refer to the crystal manufacturer's specifications for the required crystal load capacitor value.

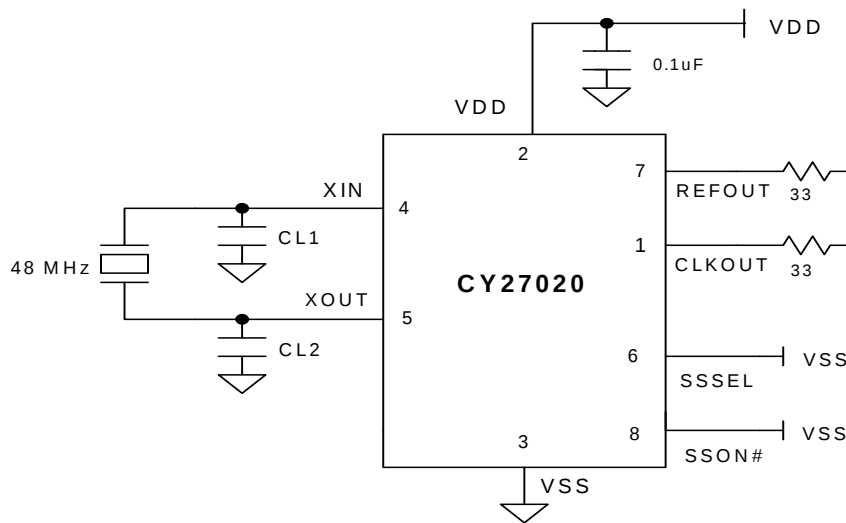
AC Electrical Specifications

($V_{DD} = 3.3 \text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to 70°C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
IFR	Input frequency range		44	48	52	MHz
t_r	Rise time [4, 5]		—	1	2	ns
t_f	Fall time [4, 5]		—	1	2	ns
SS%	Spread spectrum percentage	SSON# = 0, SSSEL = 0	—	-1	—	%
		SSON# = 0, SSSEL = 1	—	-3	—	%
t_{PU}	Power-up to stable output ^[6]	All output clocks	—	—	3	ms
t_{DC}	Clock duty cycle [4, 6]	CL = 15 pF	45	50	55	%
t_{CCJ}	REFOUT cycle-to-cycle jitter [4, 6]	CL = 15 pF	—	—	350	ps
	CLKOUT cycle-to-cycle jitter [4, 6]		—	100	250	ps

Application Schematic Example

Figure 3. Application Schematic Example [7, 8]



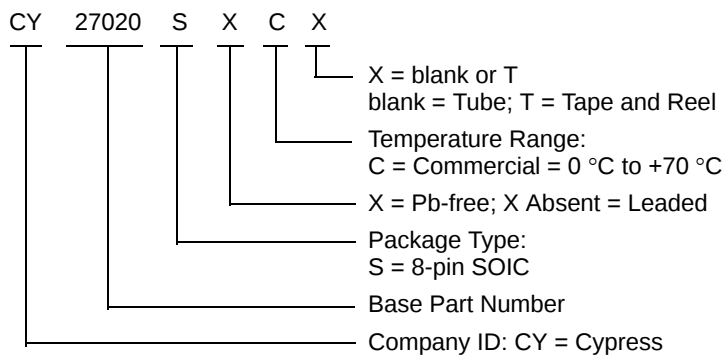
Notes

- Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs. All outputs loaded with 15 pF.
- Measured between $0.1 \times V_{DD}$ and $0.9 \times V_{DD}$ volts.
- Triggering is done at 1.5 V.
- The circuit shows -1.0% spread. Refer to [Frequency Table on page 1](#) for details.
- Use the crystal manufacturer's recommended values for CL1 and CL2 load capacitors.

Ordering Information

Part Number	Package Type	Production Flow
Pb-free		
CY27020SXC	8-pin SOIC	Commercial, 0 °C to 70 °C
CY27020SXCT	8-pin SOIC - Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions

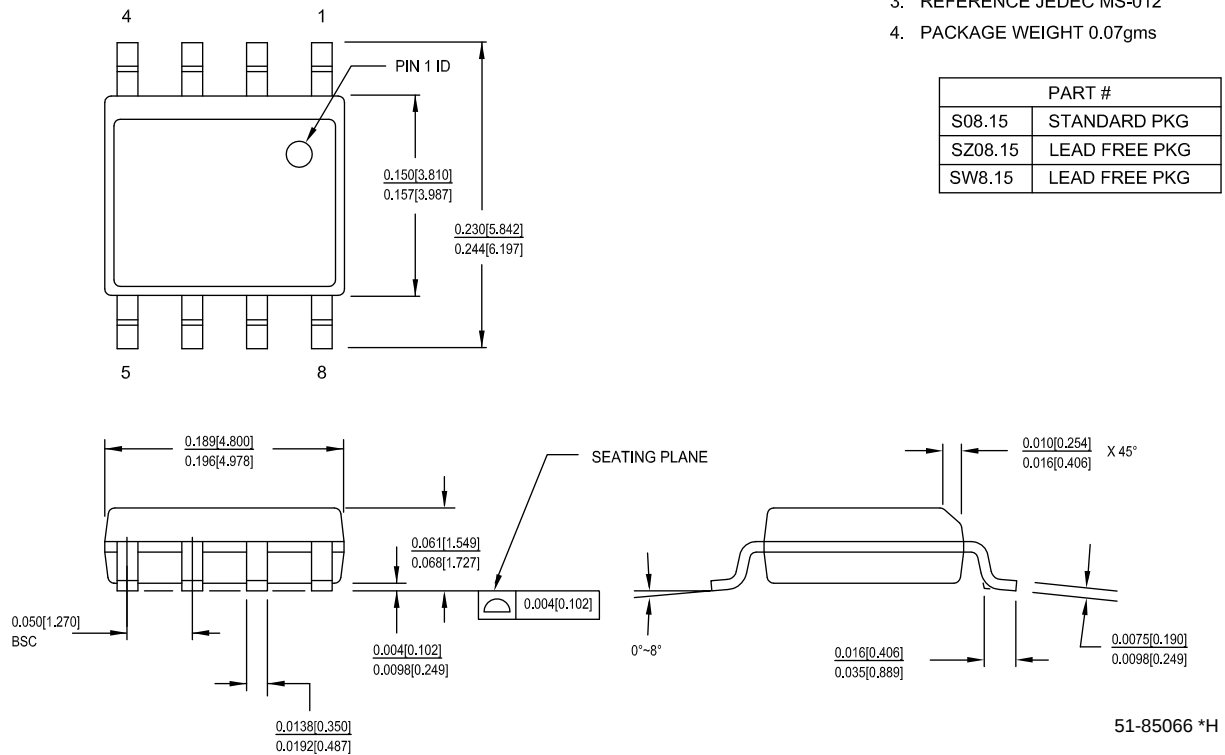


Package Drawing and Dimension

Figure 4. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
MAX.
2. PIN 1 ID IS OPTIONAL,
ROUND ON SINGLE LEADFRAME
RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
CLKOUT	Reference Clock Out
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
PD	Power Down
PLL	Phase Locked Loop
PPM	Parts Per Million
SS	Spread Spectrum
SSC	Spread Spectrum Clock
SSCG	Spread Spectrum Clock Generation
SSON	Spread Spectrum ON

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY27020, Spread Spectrum Clock Generator Document Number: 38-07273				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	110661	02/19/02	XHT	New data sheet.
*A	122868	12/21/02	RBI	Add power up requirements to maximum rating information
*B	279429	See ECN	RGL	Added Lead-free Devices
*C	2759365	09/02/2009	TSAI	Updated template. Post to external web.
*D	2899304	03/25/2010	CXQ	Removed inactive parts from Ordering Information Updated Package Drawing and Dimension .
*E	3041840	09/29/2010	CXQ	Removed "IC" from end of document title. Fixed various formatting and typographical errors. Change all SSON pin references to SSON#. Added row to Table 1 for explicit select pin functional explanation. Removed references to Cera-lock input. Removed redundant Note 3.
*F	4162220	10/16/2013	CINM	Updated Package Drawing and Dimension : spec 51-85066 – Changed revision from *D to *F. Updated in new template. Completing Sunset Review.
*G	4587350	12/05/2014	AJU	Added related documentation hyperlink in page 1.
*H	5507104	11/02/2016	PAWK	Updated the template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2002-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Cypress Semiconductor:

[CY27020SXC](#) [CY27020SXCT](#)