



THIS SPEC IS OBSOLETE

Spec No: 001-08350

Spec Title: CY7C1061DV18, 16-MBIT (1M X 16) STATIC RAM

Replaced by: None

Features

- High Speed
 - $t_{AA} = 15 \text{ ns}$
- Low Active Power
 - $I_{CC} = 150 \text{ mA}$ at 67 MHz
- Low complementary metal oxide semiconductor (CMOS) Standby Power
 - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of 1.7 V to 2.2 V
- 1.5 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 and CE_2 features
- Available in Pb-free 54-pin thin small outline package (TSOP) Type II package

Functional Description

The CY7C1061DV18 is a high performance CMOS Static RAM (SRAM) organized as 1,048,576 words by 16 bits.

To write to the device, enable the chip (\overline{CE}_1 LOW and CE_2 HIGH) while forcing the Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

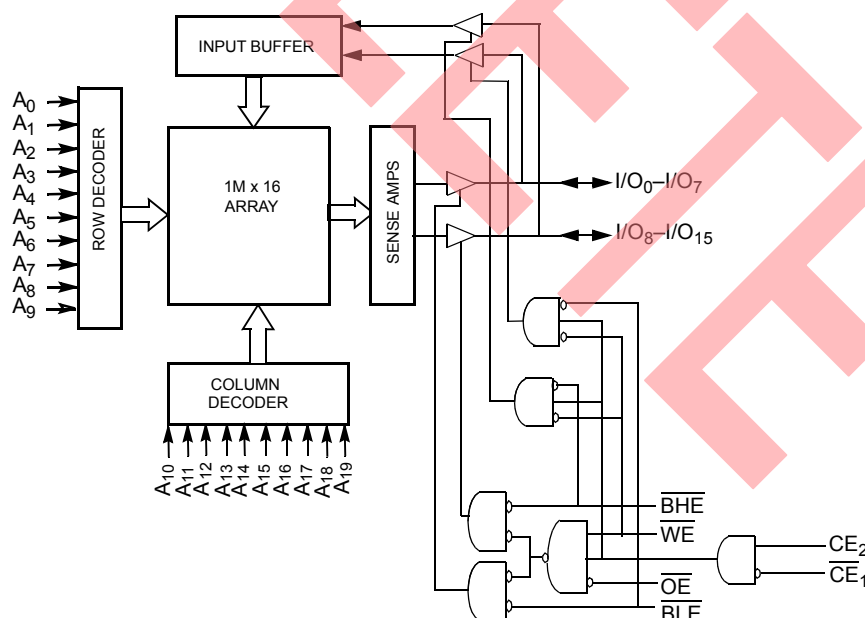
To read from the device, enable the chip by taking \overline{CE}_1 LOW and CE_2 HIGH while forcing the Output Enable (\overline{OE}) LOW and the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the [Truth Table on page 11](#) for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH/ CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a Write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

The CY7C1061DV18 is available in a 54-pin TSOP II pinout.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



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Selection Guide

Description	-15	Unit
Maximum access time	15	ns
Maximum operating current	150	mA
Maximum CMOS standby current	25	mA

Pin Configurations

Figure 1. 54-pin TSOP II pinout (Top View)

I/O ₁₂	1	54	I/O ₁₁
V _{CC}	2	53	V _{SS}
I/O ₁₃	3	52	I/O ₁₀
I/O ₁₄	4	51	I/O ₉
V _{SS}	5	50	V _{CC}
I/O ₁₅	6	49	I/O ₈
A ₄	7	48	A ₅
A ₃	8	47	A ₆
A ₂	9	46	A ₇
A ₁	10	45	A ₈
A ₀	11	44	A ₉
BHE	12	43	NC
CE ₁	13	42	OE
V _{CC}	14	41	V _{SS}
WE	15	40	NC
CE ₂	16	39	BLE
A ₁₉	17	38	A ₁₀
A ₁₈	18	37	A ₁₁
A ₁₇	19	36	A ₁₂
A ₁₆	20	35	A ₁₃
A ₁₅	21	34	A ₁₄
I/O ₀	22	33	I/O ₇
V _{CC}	23	32	V _{SS}
I/O ₁	24	31	I/O ₆
I/O ₂	25	30	I/O ₅
V _{SS}	26	29	V _{CC}
I/O ₃	27	28	I/O ₄

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage
on V_{CC} to relative GND ^[1] -0.2 V to +2.45 V

DC voltage applied to outputs
in High Z state ^[1] -0.2 V to +2.45 V

DC input voltage ^[1] -0.2 V to +2.45 V

Current into outputs (LOW) 20 mA

Static discharge voltage
(per MIL-STD-883, method 3015) >2001 V

Latch-up current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	-40 °C to +85 °C	1.7 V to 2.2 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC} , $I_{OH} = -0.1$ mA	1.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC} , $I_{OL} = 0.1$ mA	–	0.2	V
V_{IH}	Input HIGH voltage		1.4	$V_{CC} + 0.2$	V
V_{IL}	Input LOW voltage ^[1]		-0.2	0.4	V
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	+1	μA
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, output disabled	-1	+1	μA
I_{CC}	V_{CC} operating supply current	Max V_{CC} , $f = f_{MAX} = 1/t_{RC}$, $I_{OUT} = 0$ mA CMOS levels	–	150	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	$\overline{CE}_1 \geq V_{IH}$, $CE_2 \leq V_{IL}$, Max V_{CC} , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	30	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, Max V_{CC} , $V_{IN} \geq V_{CC} - 0.2$ V, or $V_{IN} \leq 0.2$ V, $f = 0$	–	25	mA

Note

1. V_{IL} (min) = -2.0 V for pulse durations of less than 20 ns.

Capacitance

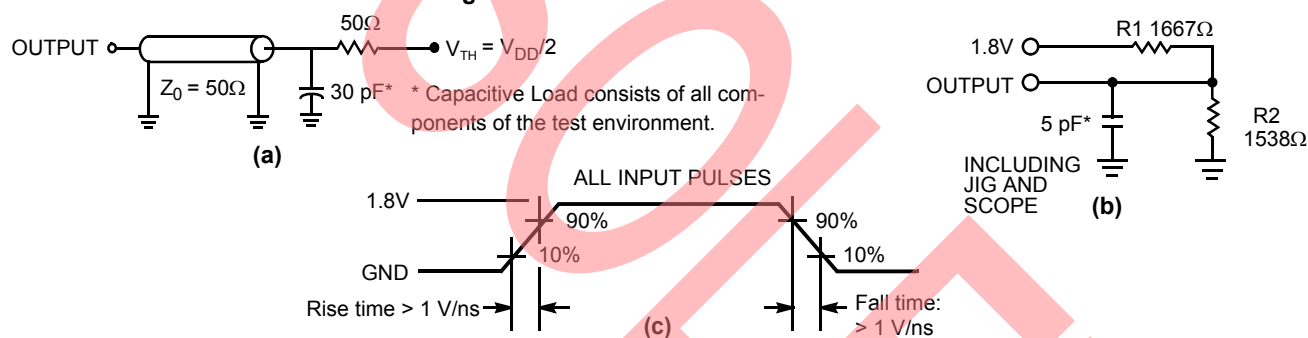
Parameter ^[2]	Description	Test Conditions	54-pin TSOP II	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 1.8\text{ V}$.	6	pF
C_{OUT}	I/O capacitance		8	pF

Thermal Resistance

Parameter ^[2]	Description	Test Conditions	54-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	76.15	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		14.15	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[3]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (1.5 V). 150 μs (t_{power}) after reaching the minimum operating V_{DD} , normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR} , 1.5 V) voltage.

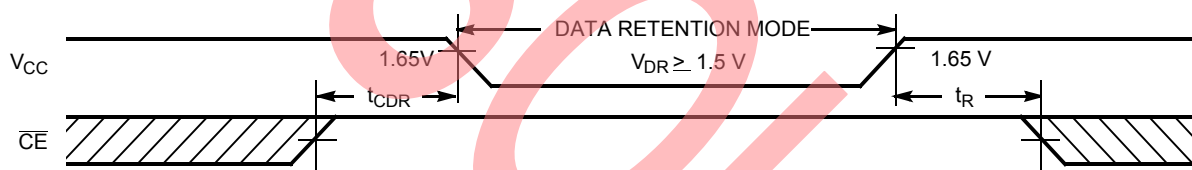
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[4]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR}	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$, $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$, or $V_{IN} \leq 0.2\text{ V}$	–	–	25	mA
$t_{CDR}^{[5]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[6]}$	Operation recovery time		t_{RC}	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^{\circ}\text{C}$.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

AC Switching Characteristics

Over the Operating Range

Parameter ^[7]	Description	-15		Unit
		Min	Max	
Read Cycle				
t _{power}	V _{CC} (typical) to the first access ^[8]	150	–	μs
t _{RC}	Read cycle time	15	–	ns
t _{AA}	Address to data valid	–	15	ns
t _{OHA}	Data hold from address change	3	–	ns
t _{ACE}	$\overline{\text{CE}}_1$ LOW/CE ₂ HIGH to data valid	–	15	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	7	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	1	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[9]	–	7	ns
t _{LZCE}	$\overline{\text{CE}}_1$ LOW/CE ₂ HIGH to Low Z ^[9]	3	–	ns
t _{HZCE}	$\overline{\text{CE}}_1$ HIGH/CE ₂ LOW to High Z ^[9]	–	7	ns
t _{PU}	$\overline{\text{CE}}_1$ LOW/CE ₂ HIGH to Power-up ^[10]	0	–	ns
t _{PD}	$\overline{\text{CE}}_1$ HIGH/CE ₂ LOW to Power-down ^[10]	–	15	ns
t _{DBE}	Byte Enable to data valid	–	7	ns
t _{LZBE}	Byte Enable to Low Z	1	–	ns
t _{HZBE}	Byte Disable to High Z	–	7	ns
Write Cycle ^[11, 12]				
t _{WC}	Write cycle time	15	–	ns
t _{SCE}	$\overline{\text{CE}}_1$ LOW/CE ₂ HIGH to write end	10	–	ns
t _{AW}	Address setup to write end	10	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ pulse width	10	–	ns
t _{SD}	Data setup to write end	7	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[13]	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[13]	–	7	ns
t _{BW}	Byte enable to end of write	10	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 0.9 V, input pulse levels of 0 to 1.8 V. Test conditions for the Read cycle use output loading shown in part a) of the [Figure 2](#), unless specified otherwise.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , and t_{LZOE} , t_{LZCE} , t_{LZWE} , t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of [Figure 2](#). Transition is measured ± 200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of $\overline{\text{CE}}_1$ LOW (CE_2 HIGH) and $\overline{\text{WE}}$ LOW. Chip enables must be active and $\overline{\text{WE}}$ and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , and t_{LZOE} , t_{LZCE} , t_{LZWE} , t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of [Figure 2](#). Transition is measured ± 200 mV from steady-state voltage.

Switching Waveforms

Figure 4. Read Cycle No. 1 [14, 15]

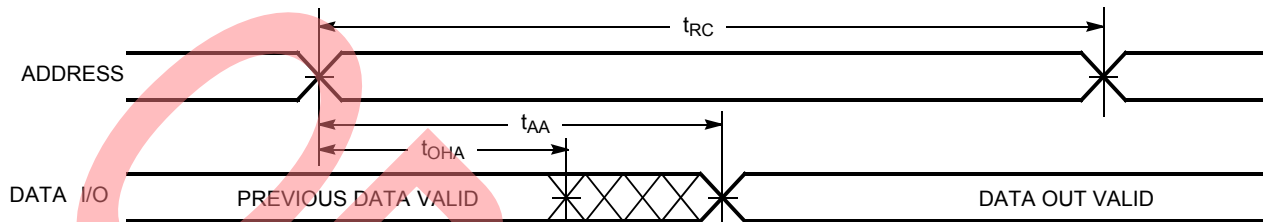
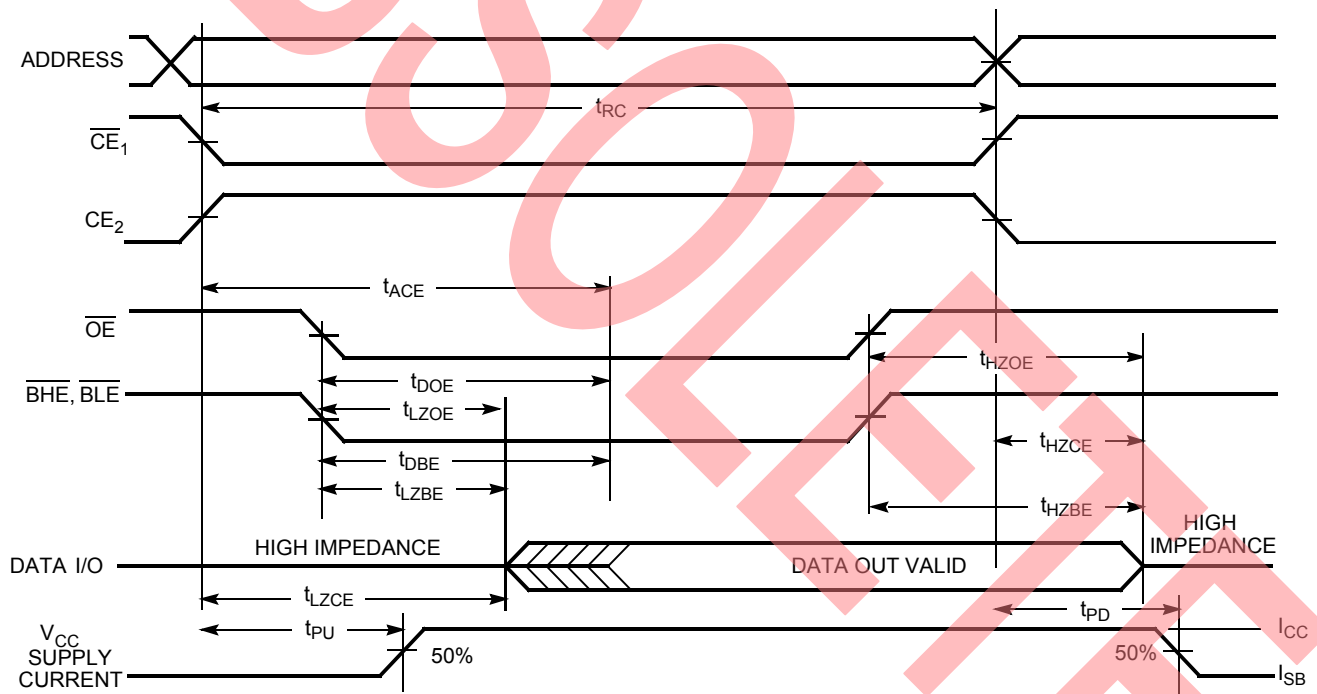


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [16, 17]



Notes

14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu s$ or stable at $V_{CC(min)} \geq 100 \mu s$.
15. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or $\overline{BLE} = V_{IL}$. $CE_2 = V_{IH}$.
16. \overline{WE} is HIGH for Read cycle.
17. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [18, 19, 20]

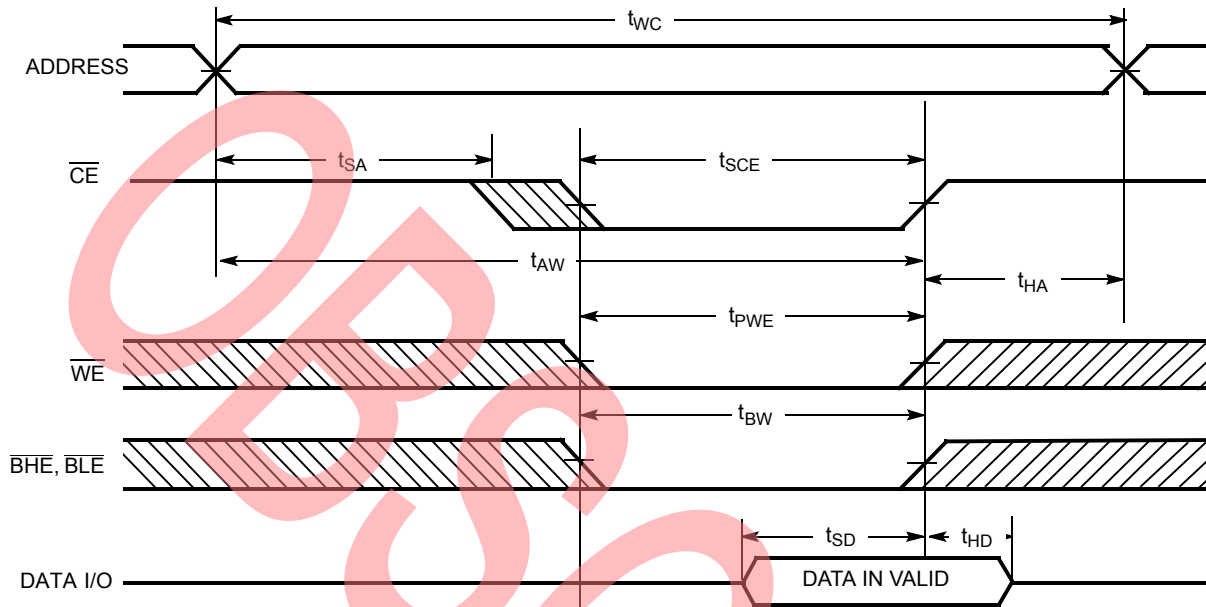
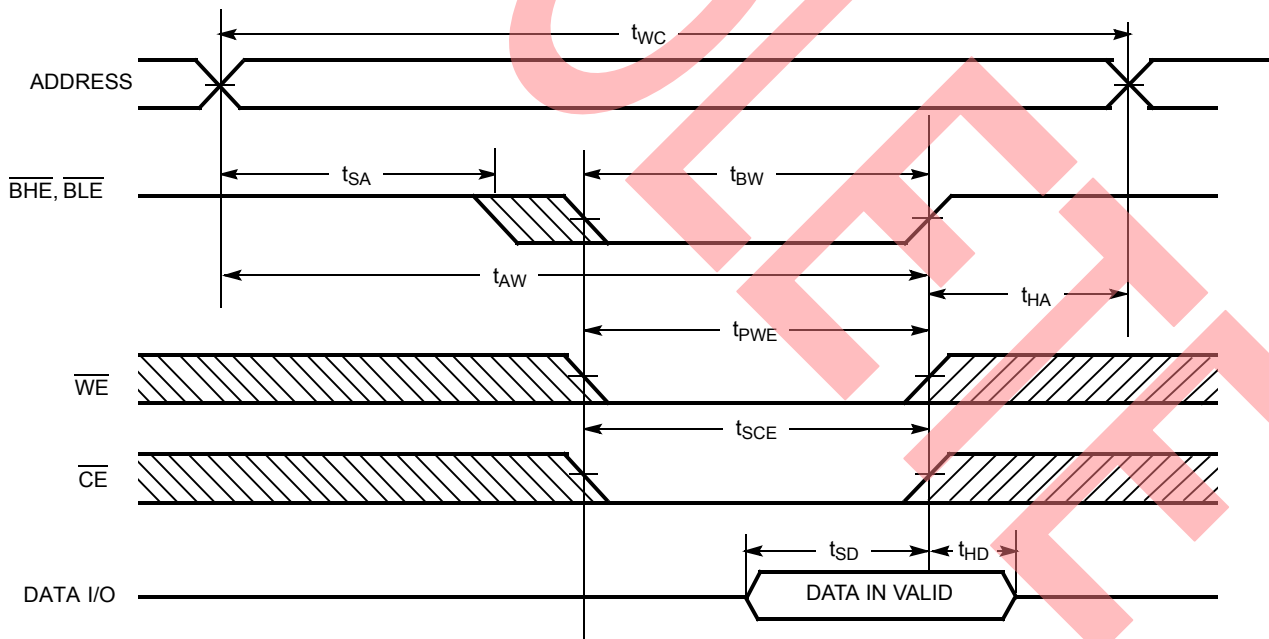


Figure 7. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes

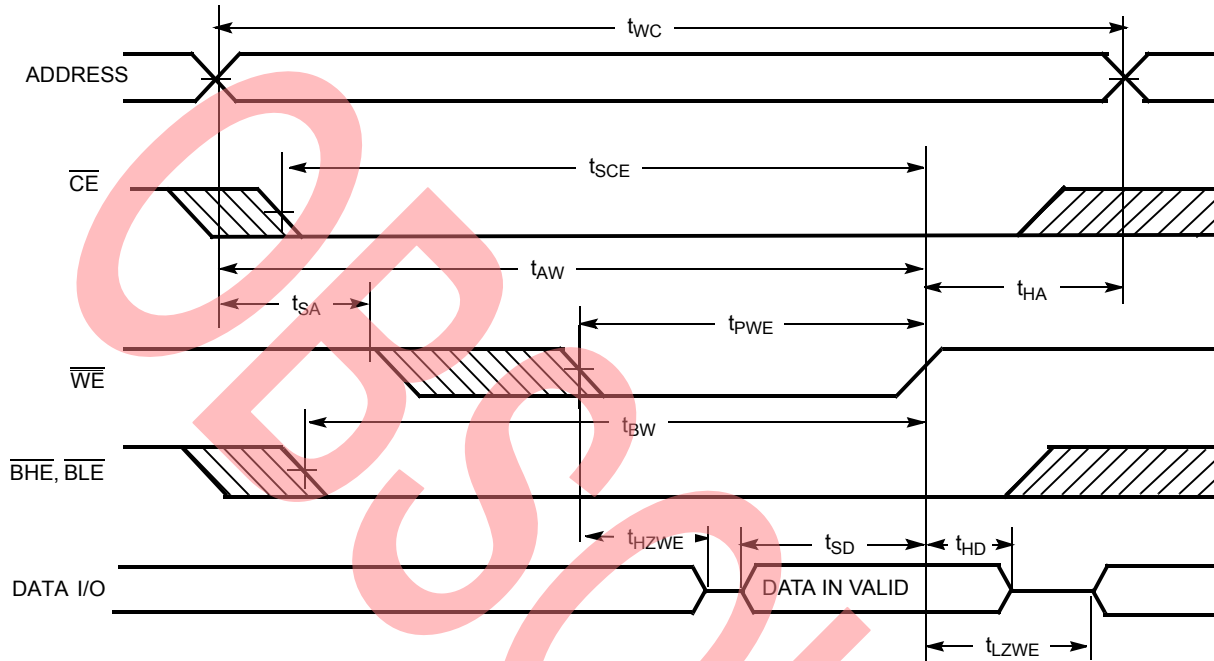
18. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.

19. If $\overline{\text{CE}}_1$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

20. $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$. When $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or $\overline{\text{CE}}_2$ is LOW, $\overline{\text{CE}}$ is HIGH.

Switching Waveforms(continued)

Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ Low) [21, 22, 23]



Notes

21. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
22. If $\overline{\text{CE}}_1$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.
23. $\overline{\text{CE}}$ is a shorthand combination of both $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ combined. It is active LOW.

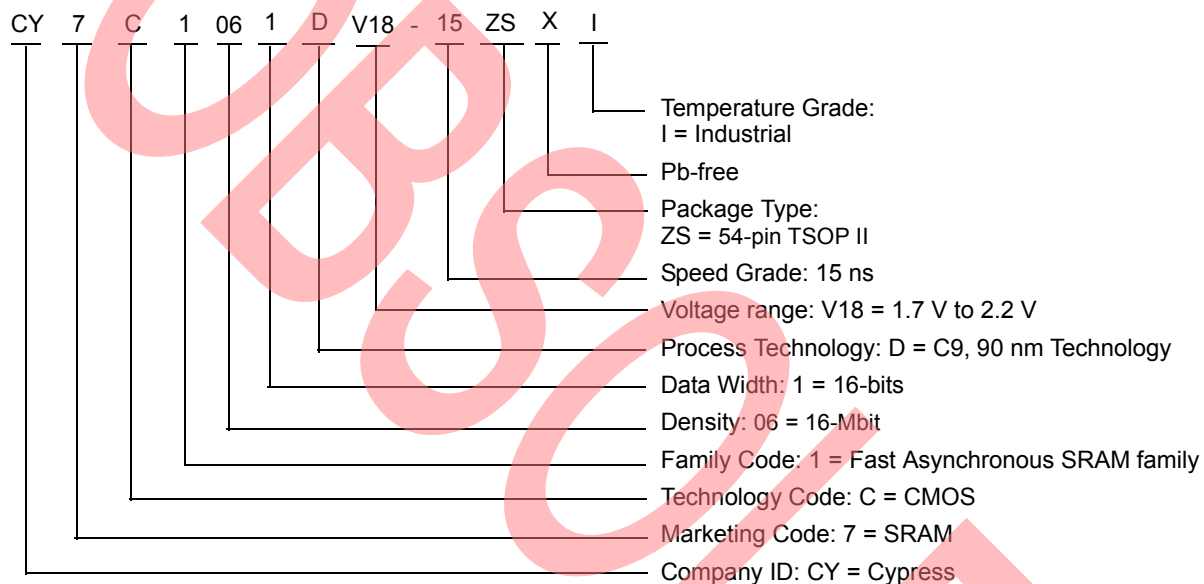
Truth Table

\overline{CE}_1	CE_2	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power-down	Standby (I _{SB})
X	L	X	X	X	X	High Z	High Z	Power-down	Standby (I _{SB})
L	H	L	H	L	L	Data out	Data out	Read all bits	Active (I _{CC})
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active (I _{CC})
L	H	L	H	H	L	High Z	Data out	Read upper bits only	Active (I _{CC})
L	H	X	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active (I _{CC})
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active (I _{CC})
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1061DV18-15ZSXI	51-85160	54-pin TSOP II (Pb-free)	Industrial

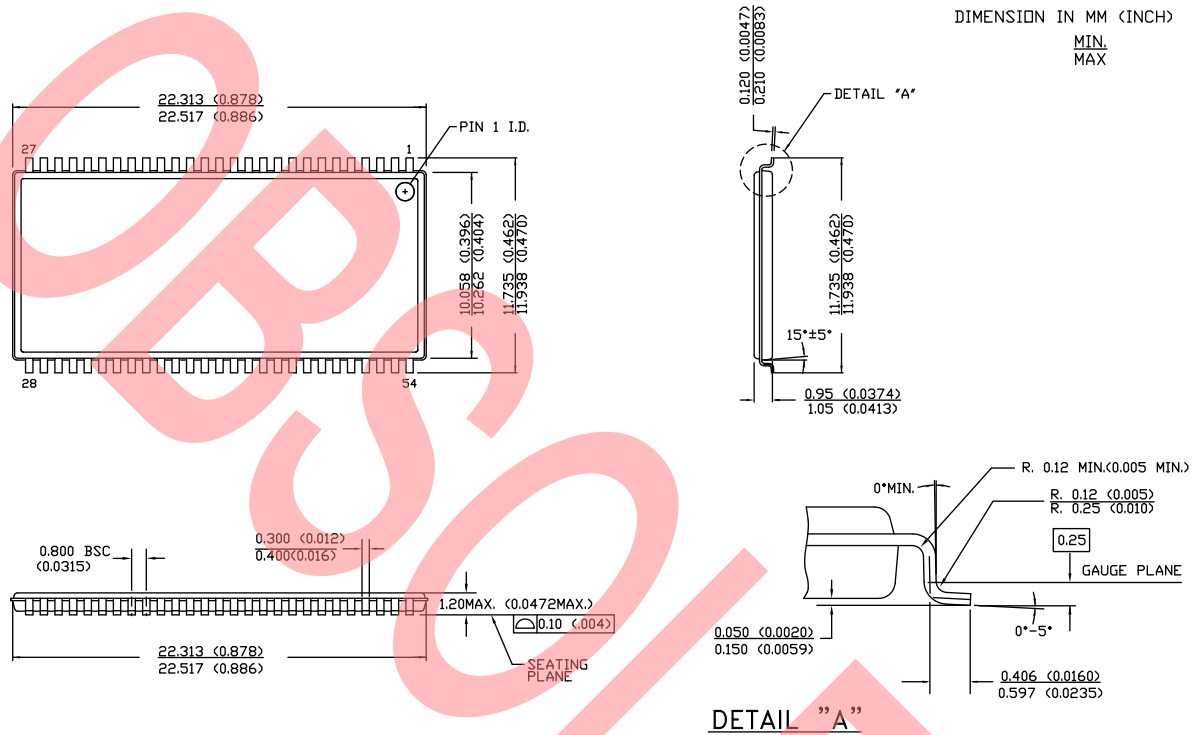
Ordering Code Definitions



Package Diagram

Figure 9. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Package Outline, 51-85160

54 Lead TSOP TYPE II – STANDARD



51-85160 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1061DV18, 16-Mbit (1M × 16) Static RAM
Document Number: 001-08350

Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	469420	See ECN	NXR	New data sheet.
*A	2761557	09/09/2009	VKN	Rearranged sections for better clarity.
*B	2800121	11/06/2009	VKN	<p>Changed status from Final to Preliminary.</p> <p>Updated Selection Guide:</p> <p>Changed value of "Maximum operating current" from 100 mA to 150 mA.</p> <p>Updated Thermal Resistance:</p> <p>Replaced TBD with values for both Θ_{JA} and Θ_{JC} parameters.</p> <p>Updated Data Retention Characteristics:</p> <p>Changed minimum value of V_{DR} parameter from 1.2 V to 1.5 V.</p> <p>Updated AC Switching Characteristics:</p> <p>Changed minimum value of t_{LZOE} parameter from 0 ns to 1 ns.</p> <p>Changed minimum value of t_{LZBE} parameter from 0 ns to 1 ns.</p> <p>Changed minimum value of t_{LZCE} parameter from 0 ns to 3 ns.</p> <p>Updated Package Diagram:</p> <p>Replaced "6 × 8 × 1 mm FBGA package" with "8 × 9.5 × 1 mm FBGA package" (Removed spec 51-85150 *D and added spec 51-85178 *A).</p>
*C	2915361	04/16/2010	VKN	<p>Changed status from Preliminary to Final.</p> <p>Removed 48-ball FBGA package related information in all instances across the document.</p> <p>Updated links in Sales, Solutions, and Legal Information</p>
*D	2923463	04/27/2010	RAME	Post to external web.
*E	3109102	12/13/2010	PRAS	Added Ordering Code Definitions .
*F	3147322	01/19/2011	PRAS	<p>Added Acronyms and Units of Measure.</p> <p>Updated to new template.</p>
*G	3387026	09/29/2011	TAVA	<p>Minor technical edits.</p> <p>Updated Package Diagram.</p>
*H	4217075	12/11/2013	MEMJ	<p>Updated Features:</p> <p>Added 48-ball VFBGA package related information.</p> <p>Updated Functional Description:</p> <p>Added 48-ball VFBGA package related information.</p> <p>Updated Pin Configurations:</p> <p>Added 48-ball VFBGA package related information.</p> <p>Updated Ordering Information (Updated part numbers).</p> <p>Updated Package Diagram:</p> <p>spec 51-85160 – Changed revision from *C to *D.</p> <p>Added 48-ball VFBGA package related information.</p> <p>Updated to new template.</p>
*I	4548836	10/22/2014	MEMJ	<p>Updated Package Diagram:</p> <p>spec 51-85160 – Changed revision from *D to *E.</p> <p>Completing Sunset Review.</p>
*J	4573121	11/18/2014	MEMJ	<p>Updated Functional Description:</p> <p>Added "For a complete list of related documentation, click here." at the end.</p>

Document History Page(continued)

Document Title: CY7C1061DV18, 16-Mbit (1M × 16) Static RAM Document Number: 001-08350				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
*K	4987892	10/26/2015	NILE	Removed 48-ball VFBGA package related information in all instances across the document. Updated Thermal Resistance : Changed value of Θ_{JA} parameter corresponding to TSOP II package from 24.18 °C/W to 76.15 °C/W. Changed value of Θ_{JC} parameter corresponding to TSOP II package from 5.40 °C/W to 14.15 °C/W. Updated Ordering Information : Updated part numbers. Updated Package Diagram : Removed spec 51-85178 *C. Updated to new template. Completing Sunset Review.
*L	5500113	10/28/2016	NILE	Obsolete document. Completing Sunset Review.

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